HIGH-SPEED ANALOG-TO-DIGITAL CONVERSION IN SIGE HBT TECHNOLOGY

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HIGH-SPEED ANALOG-TO-DIGITAL CONVERSION IN SIGE HBT TECHNOLOGY

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To my beloved family

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SUMMARY

The objective of this research is to explore high-speed analog-to-digital converters (ADCs) using silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) for wireless digital receiver applications. The stringent requirements of ADCs for the high-performance next-generation wireless digital receiver include (1) low power, (2) low cost, (3) wide input signal bandwidth, (4) high sampling rate, and (5) medium to high resolution. The proposed research achieves the objective by implementing high-performance ADC's key building blocks and integrating these building blocks into a complete sigma-delta analog-to-digital modulator that satisfies the demanding specifications of next-generation wireless digital receiver applications. All circuits are implemented in SiGe BiCMOS technology. The scope of this research is divided into two main parts: (1) high-performance key building blocks of the ADC, and (2) high-speed sigma-delta analog-to-digital modulator. The research on ADC's building blocks includes the design of two high-speed track-and-hold amplifiers (THA) and two wide-bandwidth comparators operating at the sampling rate > 10 GS/sec with satisfying resolution. The research on high-speed sigma-delta analog-to-digital modulator includes the design and experimental characterization of a high-speed second-order low-pass sigma-delta modulator, which can operate with a sampling rate up to 20 GS/sec and with a medium resolution.

The research is envisioned to demonstrate that the SiGe HBT technology is an ideal platform for the design of high-speed ADCs.

Details of this dissertation can be found in the following referred publications:

1. High-Speed Comparators (Chapter II, also published in [66] [67]).

2. Track-and-Hold Amplifiers(Chapter III, also published in [76] [77]).

3. A high-speed second-order low-pass sigma-delta modulator(Chapter IV, also published in [88]).

CHAPTER I

INTRODUCTION

1.1 Analog-to-Digital Converters for Wireless Digital Receiver

The last three decades have seen the deployment of signal processing systems with constantly increasing performance and sophistication, benefiting from the rapid advances of digital integrated circuit technologies. In these systems, a wide variety of continuous-time signals, including speech, image, instrumentation, and wire/wireless communications, are converted into digital signals on which very large scale integrated (VLSI) digital circuitry performs the bulk of complex signal and data manipulation. In the process of signal conversion, the analog-to-digital converter (ADC) is a key component in determining the overall performance of those signal processing systems, this is especially true in the scenario of wireless digital receivers targeting civilian, commercial, and military applications [1].

Traditionally, the superheterodyne architecture with double down-conversion stages has been a popular option in the design of a wireless digital receiver [2]. However, the drawbacks of the superheterodyne architecture restrict the receiver's performance improvement: the analog down-conversion stages will introduce distortion, require considerable calibration, and result in a bulky, costly, and temperature-sensitive receiver [3].

One of the effective solutions to those problems is to reduce or completely eliminate the analog down-conversion stages, push the digital interface and ADC closer to the sensor/antenna, and finally get a direct-conversion or zero-IF architecture for the wireless digital receiver [4]. In addition to the advantages of physical size, power

consumption and cost, another benefit achieved in the zero-IF architecture is the improved tunability/programmability of the receiver, because of the increased working load processed in the digital part of the system. For example, the suppression of interfering signals is significantly enhanced through digital filtering and beam forming [5]. Figure 1 shows three different architectures of the wireless digital receiver with different structure complexity.

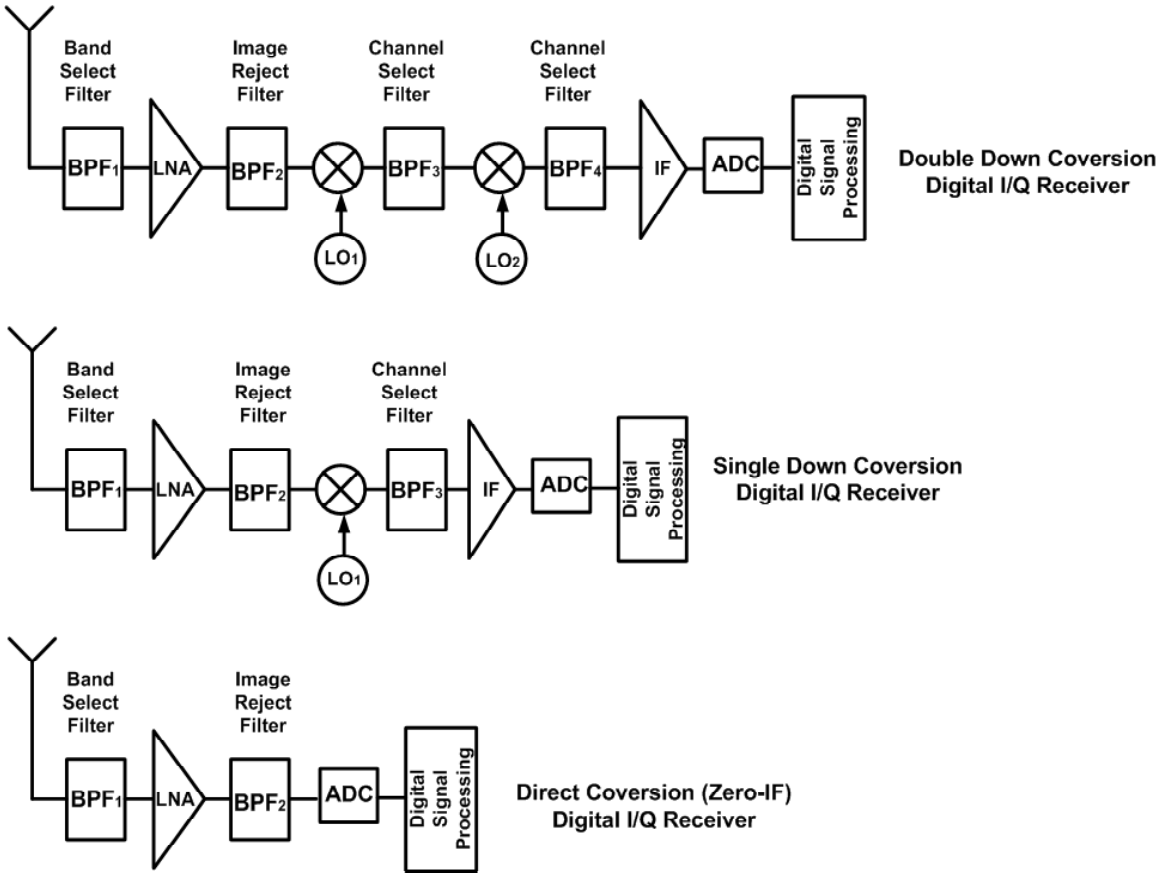

Figure 1: Migration of ADC toward the antenna in the digital receivers.

With the ADC migrating closer toward the antenna, signal digitization over a wide frequency spectrum from the low intermediate frequency (IF) to the high IF, and even at the radio frequency (RF) in some applications, is required for the ADC. Serious

performance demands on the resolution, sampling rate, bandwidth and dynamic range are placed on the ADC used in the digital receiver of this type.

For example, for the stressing mission in the electronic warfare (EW), advanced electronic support measure (ESM) receivers are needed to meet the specific requirements and are expected to have the characteristics of broad instantaneous bandwidth (>1 GHz), wide spatial field-of-view, simultaneous signal processing capability, and good sensitivity and dynamic range [6]. Some limitations exist in traditional ESM receivers and need to be overcome. Those limitations include high cost, large physical size, limited programmable flexibility resulting from fixed analog hardware architecture, and analog components' tendency to drift with time and temperature. To mitigate those problems, pushing the ADC closer to the antenna and eliminating as many analog components as possible is a trend for the design of next-generation ESM receivers. The ADC that can meet the requirements of this ESM receiver should have the capability of sampling the input signal with bandwidth greater than 3 GHz and achieving a dynamic range larger than 60 dB (> 10 bits) [7].

Another example for application in military avionics is next-generation communication receiver for communication navigation and identification (CNI), whose functions include data links, SATCOM, navigation, and landing. Because of the considerations of cost, size, weight and power consumption, it is desirable to develop a common CNI receiver that can cover the entire CNI's frequency band from 30 MHz to 2 GHz. The ADC used in this receiver will be required to be capable of sampling the 20+ MHz bandwidth signal with 14 to 16 bit resolution and 120 dBm dynamic range [7]. The advantages of migrating the ADC closer toward the antenna are equally applicable to the CNI receiver.

Another application in which the high-performance ADC plays a major role is the software-defined radio(SDR), which is generating widespread interest in the telecommunication industry. With a large amount of working load being processed in the

Table 1: Estimated Availability of Future ADCs for Military Avionics (after [7], estimates made in the year of 1998).

Application	Bandwidth/ Sampling Frequency	Dynamic Range	Estimated Availability
CNI	25 MHz / > 75 Msps	100 dB (> 16 bits)	2010
CNI	100 MHz / 200 Msps	>125 dB (>20 bits)	> 2022
EW	1 GHz / 3 Gsps	60 dB (>10 bits)	2008
radar	60 MHz / 4 Gsps	60 - 80 dB (10 - 13 bits)	1999-2003
radar	200 MHz / 10 Gsps	100 dB (> 16 bits)	2008-2018
radar	200 MHz / >> 10 Gsps	120 dB (> 20 bits)	> 2018

digital part of the system, multi-mode SDR, which is capable of operating on a variety of different mobile radio standards, represents an extremely powerful tool for the evolution of future cellular systems [8]. In a multi-mode digital receiver, the ADC must be able to sample signals belonging to various standards, tailoring different sampling rate, bandwidth, dynamic range and linearity requirements, depending on the application. Dual-mode ADCs with a combination of sigma-delta and pipelined architectures have been developed to meet the different requirements on bandwidth and resolution levels set by various standards [9] - [12].

However, with the limitations of the semiconductor process and circuit technique, a gap between the performance of ADCs and requirements of SDR still exists, and the ADCs that can satisfy those demanding specifications of next-generation wireless digital receivers are yet to be developed. Table 1 shows the estimates for the future availability of the state-of-the-art ADCs that can be used in next-generation wireless digital receivers for various applications [7].

1.2 Architectures and State of the Art of High-Speed ADCs

A large variety of ADCs exist in today's market, covering a broad range of performance specifications in resolution, bandwidth, power consumption, and architecture. The ADCs can be classified into two groups in terms of sampling methods: Nyquist-rate ADC and oversampling ADC. There are several popular sub-categories in the architecture of Nyquist-rate ADC, such as flash ADC, successive approximations ADC, and pipelined ADC [13]. The sigma-delta ADC is classified into the category of oversampling ADC.

Flash ADCs are ideal for applications requiring very large bandwidth. Since the conversion occurs in a single clock cycle, the flash ADC has the advantage of being very fast. Extremely high-speed flash ADCs have been developed in recent years [15] - [20], with a 40 giga-samples per second (GS/s) sampling rate, 3-bit resolution, and 12 GHz bandwidth achieved [15]. The disadvantage of the flash architecture is that it requires a large number of comparators that are carefully matched and properly biased to achieve the linear results. Consequently, the restrictions on physical integration and input loading limit the flash ADC's resolution to a maximum of 8 bits. The flash ADC's huge power consumption also restricts its application areas significantly, especially for mobile digital systems. Figure 2 shows a 3-bit ADC with flash architecture.

Unlike the flash ADC, a pipelined converter divides the conversion task into several consecutive stages and acquires the input analog signal with a track-and-hold amplifier (THA) in the first stage. As a result of stage division, the total comparators, as well as the power consumption, can be reduced dramatically at the cost of lower conversion rate for the ADC because of the increased number of conversion cycles compared to the flash architecture.

The pipelined ADC has become a popular option for the ADC architecture for

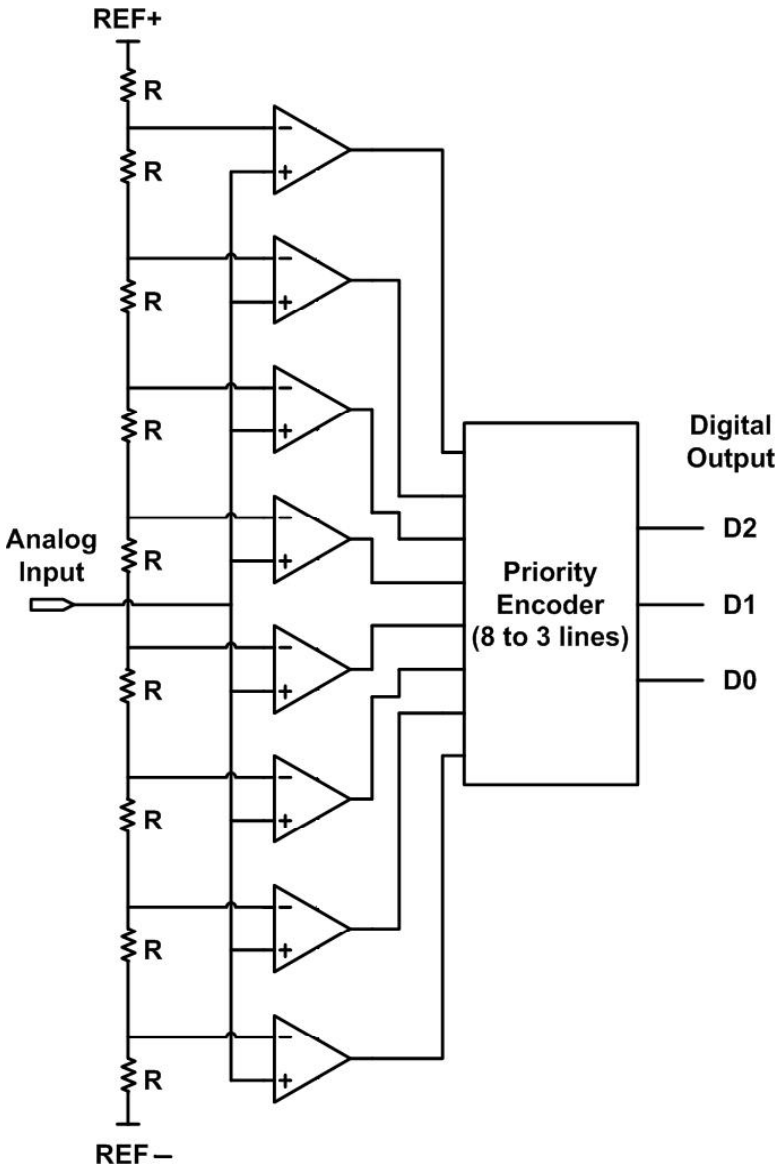

Figure 2: A 3-bit flash ADC.

sampling rates from a few mega-samples per second (MS/s) [21] [22] up to GS/s [23] - [25], with resolutions from 8 bits at the faster sampling rates [23] up to 16 bits at the lower rates [21]. These kinds of resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receiver, base station, digital video (e.g., HDTV), xDSL, cable modem, fast Ethernet, and even wide-bandwidth oscilloscope.

The sigma-delta architecture, as shown in Figure 3 for the basic block diagram,

takes a fundamentally different approach from those outlined above [26]. The basic idea behind the sigma-delta ADC is to achieve a high-resolution analog-to-digital

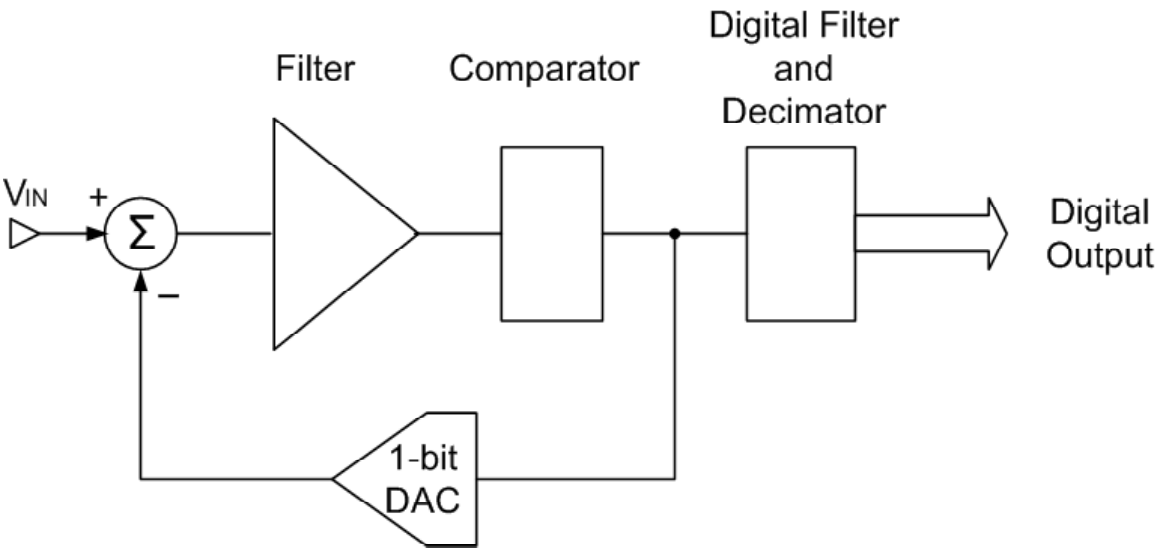

Figure 3: Block diagram of a sigma-delta ADC.

conversion through oversampling the input signal, i.e., samples are acquired from the analog waveform at a rate significantly faster than the Nyquist rate. The oversampling reduces the quantization noise power in the signal band by spreading a fixed quantization noise power over a bandwidth much larger than the signal band. Noise shaping further attenuates this noise in the signal band and amplifies it outside the signal band. In other words, the sigma-delta ADC achieves a high-resolution conversion by pushing the quantization noise power from the signal band to other frequency bands [26].

One significant advantage of this method is that analog signals are converted using only a 1-bit ADC and other analog hardware with a precision usually much lower than the resolution of the overall converter. Consequently, the design requirements can be relaxed for the individual building blocks of the whole system, and the system's power consumption can be kept at a very low level.

The sigma-delta ADC has been very attractive in applications where power consumption is a serious limiting factor and where high-resolution ADCs are needed to sample the narrow band input signals, e.g., IEEE 802.11x, Bluetooth, CDMA, GSM/GPRS/EDGE, and digital AM/FM radio [27] - [32].

The majority of sigma-delta ADCs reported to date have been implemented in the form of a z-domain discrete-time (DT) system with a switched-capacitor (SC) network in CMOS technology. Extremely high resolution (24 bits) and fairly low power can be achieved with those DT SC ADCs [33] - [36]. However, the DT SC ADC restricts the maximum sampling rate to a level much lower than what current CMOS technology can provide because of the limited unity-gain bandwidth of the operational amplifiers designed with the SC networks [37]. Continuous-time modulators can improve the sampling rate significantly and sample the input signal with a much wider bandwidth and thus are more popular in RF/IF conversion. In recent years, high-speed continuous-time $\Sigma\Delta$ AD modulators have been developed with CMOS, III-V, and SiGe technologies [32] [38] - [46]. With the technical advance of the semiconductor process and circuit design technique, $\Sigma\Delta$ AD modulators with more robust performance can be implemented to meet the demanding specifications of next-generation wireless digital receivers for civilian, commercial, and military applications.

Figure 4 shows the conversion rate versus resolution for various ADC architectures.

1.3 SiGe HBT BiCMOS Technology

In 1957, Dr. H. Kroemer introduced the theoretical foundation leading to the modern SiGe BiCMOS technology [47]. He proposed that the energy bandgap could be altered through alloy grading and carrier transport can be sped up in this way. In a graded-base SiGe HBT, a Ge concentration gradient is distributed across the base, with a higher Ge distribution at the collector side. The alloy grading of Ge alters

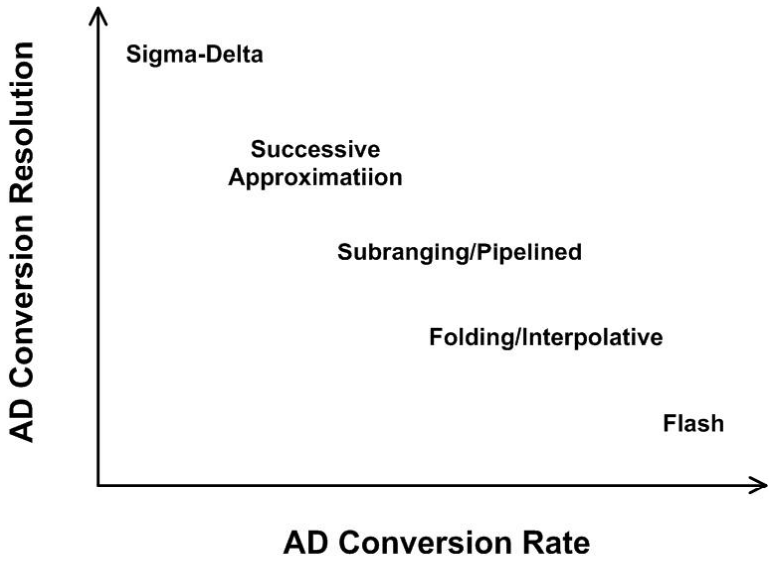

Figure 4: Conversion rate versus resolution for various ADC architectures.

the band structure and a corresponding quasi-electric field aids electron transport across the base. Compared to the conventional Si technology, SiGe technology has some characteristics that facilitate its wide applications: a) a 100% compatibility with pure Si technology, b) the speed performance significantly enhanced over conventional Si bipolar transistors, and c) further performance enhancement that can be achieved by scaling.

In recent years, rapid technological advances in the field of SiGe HBT technology make it possible to design millimeter-wave integrated circuits with high-performance HBTs while allowing a high integration of analog and digital parts, by simultaneously maintaining the HBT's strict compatibility with conventional low-cost, high-volume Si CMOS manufacturing [48] [49].

Bandgap-engineering is utilized in SiGe HBTs to dramatically improve the HBT's performance over that of traditional Si bipolar junction transistors (BJTs) in terms of current gain (β) and base transit time (τ_b), which determines the unity current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) [49].

Three generations of SiGe HBT technology are now commercially available, with

the highest f_T/f_{max} up to 200/280 GHz [50] - [52]. The fourth-generation SiGe HBT technology is under development and can achieve a remarkable f_T over 350 GHz [54] [55]. The key specifications of IBM Microelectronics' SiGe BiCMOS technologies are shown in Table 2.

Table 2: Key Specifications of SiGe HBT (*npn*) BiCMOS Technologies Offered by IBM Microelectronics.

IBM Technology	5HP/6HP [50]	7HP [51]	8HP [52]	9T [54]
HBT Generation	First	Second	Third	Fourth
f_T (GHz)	47	120	200	350
f_{max} (GHz)	65	100	280	170
BV_{CEO} (V)	3.3	1.8	1.7	1.4
$W_{E,eff}$ (μm)	0.42	0.18	0.13	0.13
CMOS L_{eff} (μm)	0.35	0.14	0.092	N/A
CMOS Supply (V)	3.3	1.8	1.5	N/A

The up-to-date SiGe HBT technology has demonstrated a comparable performance with the best-of-breed III-V compound semiconductor technologies, and thus can take over many applications traditionally dominated by the III-V technologies, e.g., 60 GHz millimeter wave transceiver [56], ultra-high-speed (40 GS/s sampling rate) ADC [15], and high-speed pattern generator ICs [57] [58]. In fact, with the attributes of high integration, high yield and low cost, SiGe products can be found in virtually all analog and high-frequency market segments, representing a very wide operating frequency range covering analog, radio frequency (RF), microwave, millimeter wave, and optical applications [59].

1.4 Organization of the Thesis

Chapter II, also published in [66] [67], presents the design of ultra-high-speed, master-slave comparators using an ECL configuration. Implemented in a commercially-available 0.18 um 120 GHz SiGe HBT BiCMOS technology, the core of the first comparator occupies a compact area of only 140 $\times$ 325 μm^2. Operating off a 3.5 V power

supply, the comparator consumes 82 mW, excluding clock and output buffers. The comparator can operate at an 18 GS/s sampling rate with a resolution of 7.1 bits, and at a 20 GS/s sampling rate with a resolution of 4.9 bits. The second comparator is implemented with a 200 GHz SiGe HBT technology, the circuit occupies an area of 0.0226 μm^2. The master-slave latches dissipates 136 mW, also from a 3.5 V power supply. Operating with an input frequency of 5 GHz, the circuit can oversample up to 32 GS/s, with the sensitivity ranging from 5 mV at 15 GS/s to 37 mV at 32 GS/s. Operating at the Nyquist rate, the comparator can sampling up to 30 GS/s, with the sensitivity ranging from 12 mV at 20 GS/s to 30 mV at 30 GS/s.

Chapter III, also published in [76] [77], presents the design of two ultra-high-speed track-and-hold amplifiers (THA) using a switched-emitter-follower (SEF) configuration. The first THA is implemented in a commercially-available 0.18 μm 120 GHz SiGe HBT BiCMOS technology, and can operate at a sampling rate of 18 GS/s with a total harmonic distortion (THD) of -32.3 dBc and a power dissipation of 128 mW, significantly smaller than other THAs in the literature operating at similar sampling rates. The second THA, implemented with a 0.13 μm 200 GHz SiGe BiCMOS technology, is an improved version compared to the first one. It can operate at 18 GS/s with a THD of -50.5 dBc.

Chapter IV, also published in [88], presents the design of a continuous-time second-order low-pass sigma-delta modulator operating at 20 GS/s. The modulator, implemented in a 0.13 μm 200 GHz SiGe HBT BiCMOS technology, achieves a signal-to-noise-ratio (SNR) of 30.5 dB over the signal band from DC to 312.5 MHz at the sampling rate of 20 GS/s, and dissipates 490 mW total power.

Chapter V will conclude the thesis and discuss possible future work.

CHAPTER II

HIGH-SPEED COMPARATORS

2.1 Introduction

The comparator is a non-linear building component of ADC, whose function is to generate a logic output of "one" and "zero" depending on the given inputs. For all high-speed ADCs, regardless of the architecture, one of the critical performance limiting building blocks is the comparator, which in large measure determines the overall performance of data converters, including the maximum sampling rate, bit resolution, and total power consumption [60]. This is particularly true in the flash and two-step ADCs, in which a large number of comparators are needed and therefore impose great constraints on the system performance of the ADC.

Monolithic high-speed comparators implemented with III-V HBTs [61][62] and SiGe HBTs [63][64] with sampling rates up to 16 GS/sec have been demonstrated. Different comparator topologies were used to satisfy the different application requirements. The comparator architecture having two differential pairs arranged in an ECL configuration [65] is favored over those in [62] and [64], because the supply voltage (power) can be lowered down and the input matching is much easier.

The ultra-high-speed comparators presented in this chapter were implemented with IBM's second-generation (7HP), and IHP's third generation (sg25c) SiGe HBT BiCMOS technology. IBM 7HP features high-performance npn SiGe HBTs with a peak f_T/f_{max} of 120/100 GHz, 0.18 μm lithography, ASIC-compatible Si CMOS devices, and a full suite of passive elements. Seven levels of metalization are available, including three levels of full copper interconnects and two thick top layer aluminum metalization layers [51]. The cross section of IBM's 120 GHz SiGe HBT is shown in

Figure 5.

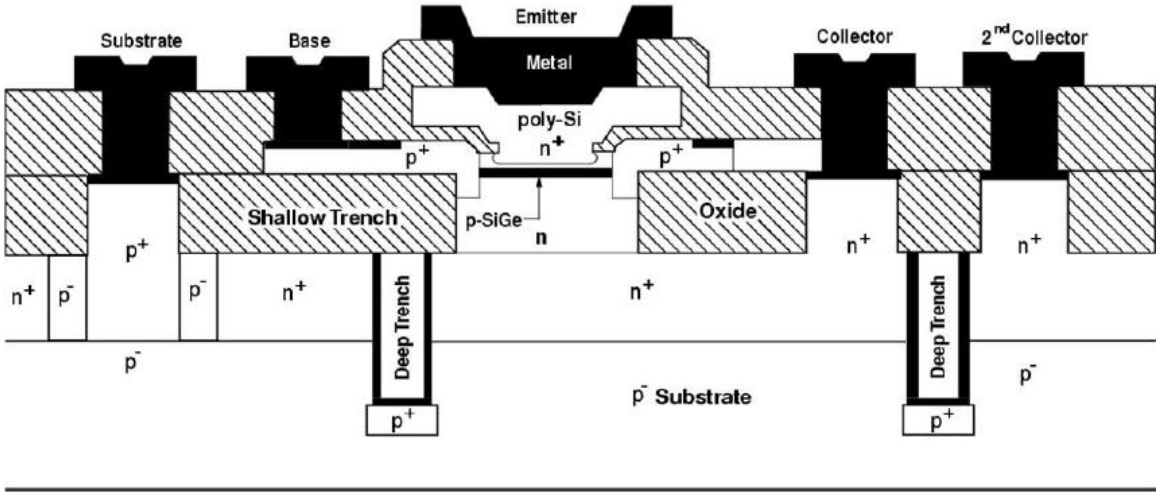

Figure 5: The cross section of IBM's 120 GHz SiGe HBT.

IHP's sg25c features high-performance npn SiGe HBTs with 200 GHz f_T/f_{max}, 0.25 μm lithography, digital CMOS devices, and a full suite of passive elements. There are several critical features on the device structure allowing the advancement in SiGe HBT performance. The whole HBT structure is formed in one active area without the shallow trench isolation between the emitter and collector contact, leading to a lower collector resistance and a reduced collector-substrate junction area. Moreover, deep trench isolation is eliminated to improve the heat dissipation and reduce the thermal resistance [53]. The cross section of IHP's 200 GHz SiGe HBT is shown in Figure 6, its parameters are summarized in Table 3.

In this chapter, two ultra-high-speed comparators using a master-slave (M/S) structure with a series gating configuration will be presented. Both comparators are well-suited for use in Nyquist and oversampling ADCs. Section 2.2 discusses some comparator design considerations, section 2.3, 2.4, and 2.5 will discuss the design, implementation, and measurement of comparator #1 and comparator #2, respectively, followed by a summary. The content in this chapter was presented at

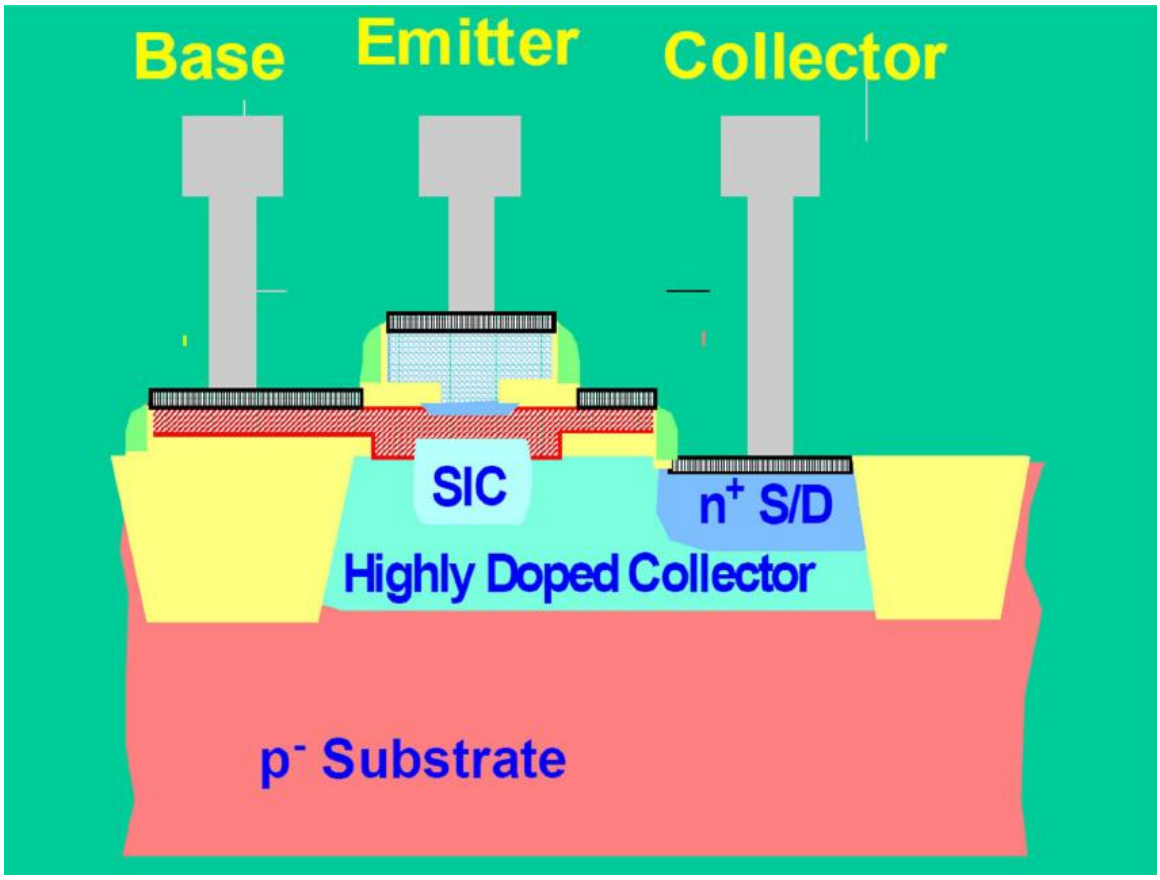

Figure 6: The cross section of IHP's 200 GHz SiGe HBT.

IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2005 [66] and Asia-Pacific Microwave Conference (APMC) 2005 [67].

2.2 Comparator Design Considerations

The block diagram of a comparator with a single latch is shown in Figure 7.

The comparator operates in track mode and latch mode with a clock controlling the mode in operation. In the track mode, the latch is disabled and the input is amplified and tracked by the preamplifier. In the latch mode, the preamplifier is disabled and the latch is enabled, the preamplifier's output is fed into the latch and is regeneratively amplified with the logic levels generated at the output.

Table 3: Summary of SG25C SiGe HBT Parameters

W_E	0.25 μm
Peak β	190
Peak f_T	200 GHz
Peak f_{max}	200 GHz
BV_{CEO}	2.0 V
$CMOSL_g$	0.25 μm
CMOS Supply	2.5 V

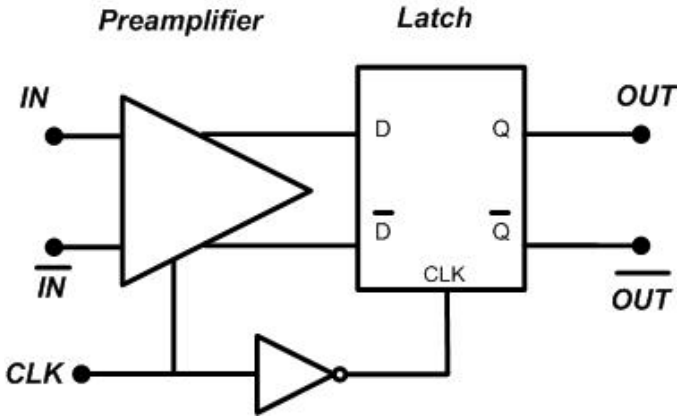

Figure 7: Block diagram of a comparator with a single latch.

The comparator design in Figure 7 suffers from the problem called "metastability" in the latch operation that may degrade the comparator's speed performance. The phenomenon arises from the presence of small inputs close to the comparator's minimum resolvable input. A latch shown in Figure 8 can be used to demonstrate the phenomenon. The latch is composed of two back-to-back amplifiers with a gain A and a time constant τ. The regeneration time T_{reg}, the time needed to generate the corresponding logic level after the latch is strobed, can be expressed as follows [13]:

$$T_{reg} = \frac{\tau}{A-1} \ln \frac{V_{x1} - V_{y1}}{V_{x0} - V_{y0}}, \tag{1}$$

where V_{x0}, V_{y0}, V_{x1}, and V_{y1} are the values of V_x and V_y at the starting and end point, respectively. There is a certain value above which V_x - V_y can be considered as a valid

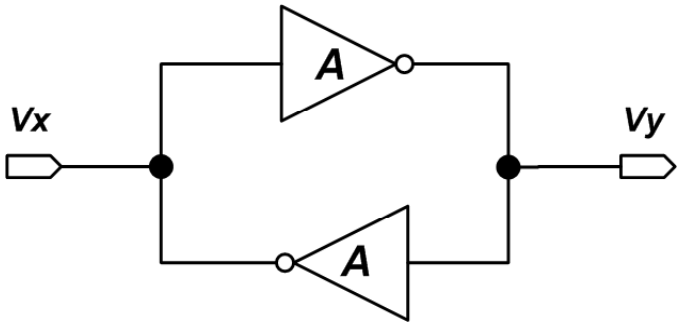

Figure 8: A latch with feedback and feedforward amplifiers.

logic level. From equation (1) it is observed that a small input V_{x0}-V_{y0} will result in a long regeneration time T_{reg}, while a large gain of the latch will reduce T_{reg}. The other two methods to reduce T_{reg} are decreasing the time constant τ or using the master-slave latch structure to increase V_{x0}-V_{y0} of the slave latch. In the design of both comparators in this chapter, the master-slave structure is utilized and special care is taken to reduce the probability of metastability.

In comparator design discussed in the following sections, the input sensitivity is defined as the minimum resolvable input. The input dynamic range is defined as the ratio between the maximum input swing and the input sensitivity, and is translated into bit accuracy using the equation:

$$Accuracy = \frac{DR - 1.76}{6.02}. \tag{2}$$

2.3 Design of High-Speed Comparator #1

This master-slave comparator is based on an ECL circuit configuration. Figure 9 shows the block diagram of the comparator, which consists of a preamplifier and a master latch driving a slave latch, followed by an output buffer. A clock buffer is used to drive the latches. A separate one-stage latch (a latching comparator without the

slave latch) was also implemented on-chip for debugging and performance comparison purposes.

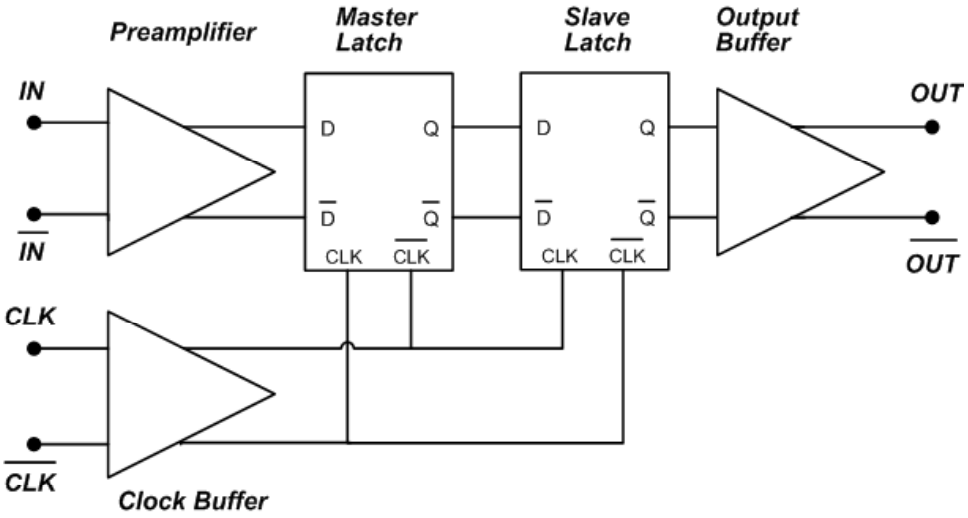

Figure 9: Block diagram of the SiGe HBT comparator.

The preamplifier, shown in Figure 10, is introduced to increase the comparator's sensitivity to the low-level input signals. The emitter-followers before and after the differential amplifier help to reduce the kick-back noise created by the switching of the latch in the following stage. The preamplifier is matched to the input source with 50 Ω pull-up resistors. Great care was taken to design the preamplifier since it plays a major role in minimizing the input offset, thus ultimately governing the comparator's resolution.

The comparator's minimum detectable input will be limited by the input-referred noise and input-referred offset, which is generated by the mismatch between the device pairs Q1/Q2, Q3/Q4, Q5/Q6, and R_{E3}/R_{E4}. The input-referred offset caused by the

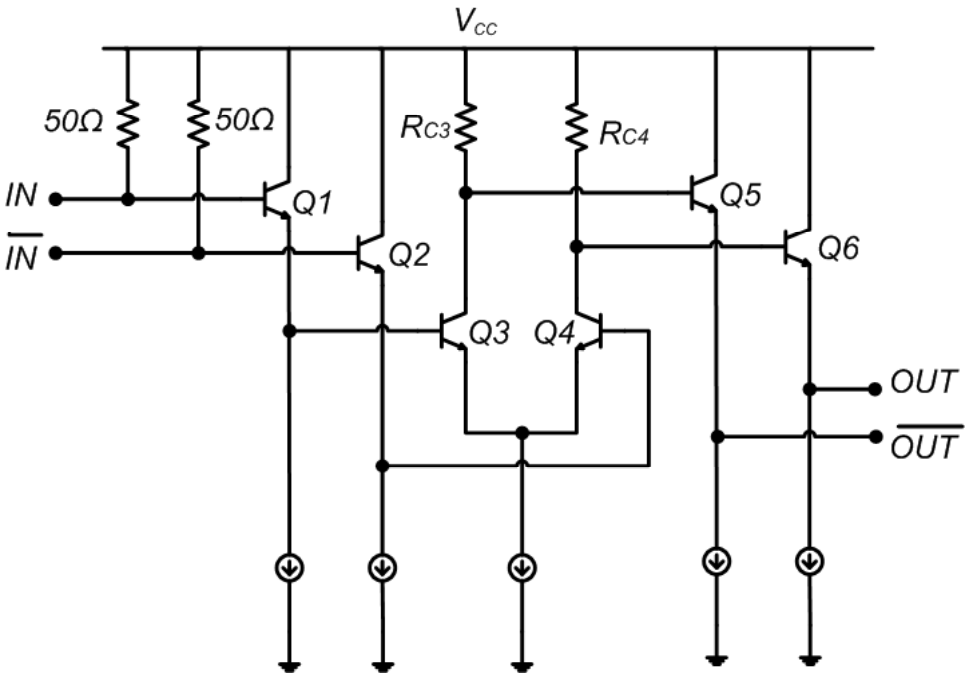

Figure 10: Schematic of the preamplifier for the SiGe HBT comparator.

mismatch in Q1/Q2, denoted as V_{BE}, can be expressed as [14]:

$$\begin{aligned} \triangle V_{BE} &= V_T \ln \frac{\triangle I_S}{I_S} \\ &= V_T \ln \frac{\triangle A}{A} \\ &\approx V_T \frac{\triangle A}{A}, \end{aligned} \tag{3}$$

where $\triangle I_S$, I_S, $\triangle A$ and A are the standard deviations and mean values of the Q1/Q2 saturation current and emitter area, respectively. Based on equation (3), it is observed that the input-referred offset is affected by both mismatch on the transistor pair and the temperature.

The input-referred offset, caused by the mismatch in all nominally identical device pairs in the preamplifier including Q1/Q2, Q3/Q4, Q5/Q6, and R_{C3}/R_{C4}, can be approximately expressed as [13]:

$$\triangle V_{offset} = V_T \ln \frac{\triangle A_{1,2}}{A_{1,2}} + V_T \ln \frac{\triangle A_{3,4}}{A_{3,4}} + \frac{1}{g_{m34} R_C} V_T \left[\frac{\triangle R_C}{R_C} + \ln \frac{\triangle A_{3,4}}{A_{3,4}} \right], \tag{4}$$

where R_C is the mean value of R_{C3} and R_{C4}, and $g_{m34}R_C$ is the voltage gain of the preamplifier differential pair. The last item could be negligible if the differential pair's voltage gain is much larger than 1, and this makes the mismatch in Q1/Q2 and Q3/Q4 a dominant contributor to the input-referred offset.

The input-referred noise arises from the thermal and shot noise of Q1/Q2 and Q3/Q4, and thermal noise of R_{C3}/R_{C4}. With all noise sources being uncorrelated, the noise special density is expressed as [13]:

$$\frac{\overline{v_n^2}}{\triangle f} = 8KT(r_{b12} + r_{e12} + r_{b34} + r_{e34} + \frac{1}{2g_{m34}} + \frac{1}{g_{m34}^2 R_C}), \tag{5}$$

where r_{b12}, r_{e12}, r_{b34}, and r_{e34} are base and emitter resistances of Q1/Q2 and Q3/Q4, respectively.

From equation (4) and (5), it is observed that an increase in voltage gain of the preamplifier will result in a decrease in both input-referred offset and noise, and hence a decrease in the comparator's minimum resolvable input.

When the input signal keeps close to the upper limit, a high current density flows through Q3 (or Q4) with Q4 (or Q3) nearly off. Long period of operation under this condition will lead to the imbalance in the thermal characteristics of Q3 and Q4, cause the thermal mismatch in the differential pair and generate undesirably large input offsets. To mitigate this problem, a large emitter size and low current density were chosen for the input transistors Q3/Q4. As observed from equation (4), larger emitter size also results in a better physical matching of the transistor pair and a lower input-referred offset, albeit with lower conversion speed as the penalty.

The schematic of latch is shown in Figure 11. In this configuration, a gate differential pair (Q7 and Q8) is loaded by a cross-coupled differential pair (Q9 and Q10) and an emitter-follower pair (Q13 and Q14). The addition of the emitter-follower pair reduces the loading effect of the following stage, speeds up the regeneration process, and increases the output voltage swing [13].

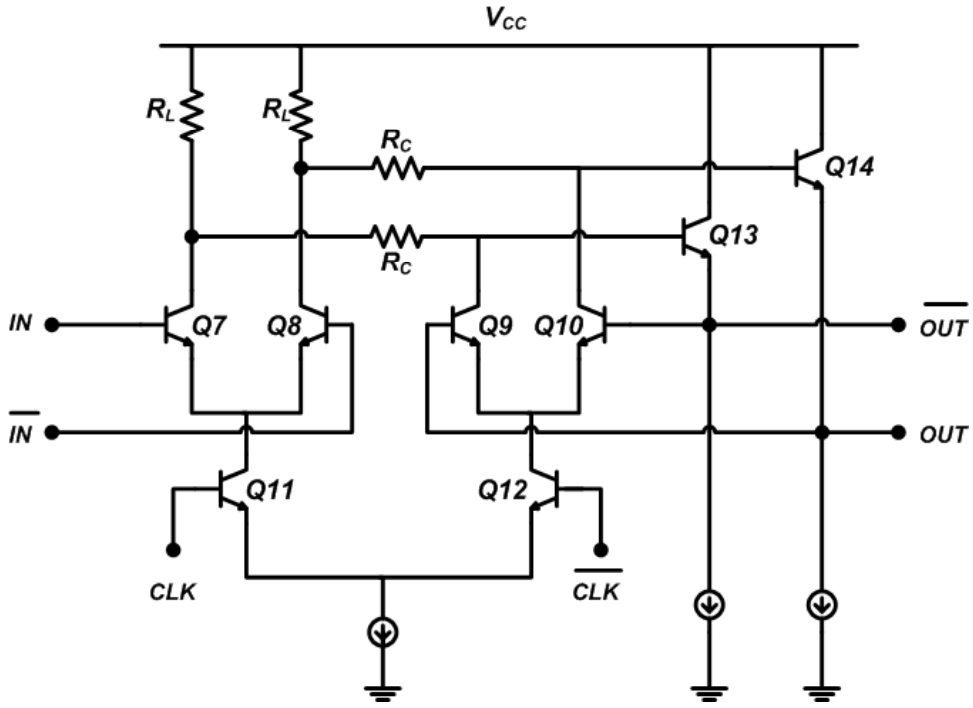

Figure 11: Schematic of the latch for the SiGe HBT comparator.

It can be shown that the regeneration response V_{out} in the latch illustrated in Figure 11 is expressed as [68]:

$$V_{out} = A_L V_{in} \exp(\frac{t}{\tau_{reg}}), \tag{6}$$

where the regeneration time constant τ_{reg} is expressed as [68]:

$$\tau_{reg} = \frac{C_\pi(r_b + R_L) + C_\mu\left[4R_L + r_b(g_m R_L + 1)\right] + C_L R_L}{g_m R_L - 1}. \tag{7}$$

For $R_L \gg r_b$, equation (7) reduces to

$$\tau_{reg} = \frac{C_{total}}{g_m}(\frac{g_m R_L}{g_m R_L - 1}), \tag{8}$$

where $C_{total} = C_\pi + C_L + 4C_\mu$.

It has been reported [68] that the dominant factor that determines a latch's overall sampling rate is the recovery time t_{rec}, which is defined as the time required by the gate differential pair's output voltage to change from a stable logic state to the midpoint

of the logic state when the latch is switching from the hold-mode to track-mode. The recovery time t_{rec} can be roughly expressed as [68]

$$t_{rec} \propto R_L \times C_{total}, \tag{9}$$

where C_{total} is the total load capacitance at the output of the gate differential pair and R_L is the load resistor, denoted in Figure 11. A large R_L will increase the recovery time whereas a small R_L will limit the output swing and degrade the slave latch's operation. A compromise can be made by adding additional collector resistors R_C, as denoted in Figure 11, to increase the gain of the latch differential pair without adversely affecting the recovery time constant. Although the additional resistors do increase the regeneration time, this side effect can be ignored because the regeneration time is not a dominant factor governing the overall sampling rate. In our design, simulations show that an 8.6 psec recovery time can be achieved using our approach and is sufficient for operation at a 20 GHz sampling rate.

Figure 12 shows a simple output buffer with two 50 Ω load resistors matched to the input impedance of the test instrumentation. A large tail current is provided to keep the voltage gain of the buffer close to unity, and a large emitter size is chosen for the transistor pair to help mitigate device self-heating.

2.4 Measurement Results of Comparator #1

The layout of the SiGe HBT comparator was made in a symmetrical fashion to minimize the effects of common-mode noise. Moreover, to reduce the parasitics associated with the interconnects, the comparator core (preamplifier + M/S latch + output buffer) was made extremely compact and occupies an area of only 140 × 325 μm^2. The overall die size, including bondpads, is 1.0 × 1.8 mm^2. The chip micrograph of the SiGe HBT comparator is shown in Figure 13.

On-wafer measurements of the comparator were performed with 40 GHz probes and cables. The comparator operates off a 3.5 V power supply and consumes only

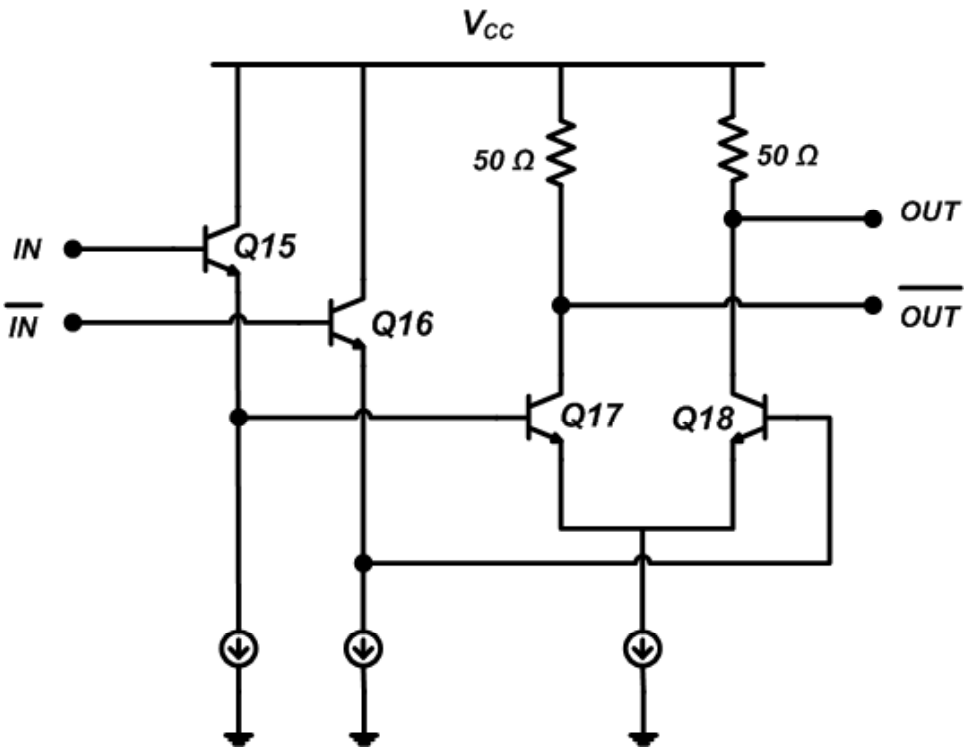

Figure 12: Schematic of the output buffer for the SiGe HBT comparator.

82 mW (preamplifier and M/S latch). Hybrids were used to split the single-ended input signals into differential signals. Since any test-setup-induced mismatch in the differential clock input will cause severe performance degradation, phase tuners were used to adjust the phase of the cables to exactly 180° phase difference after passing through the hybrid. For accurate measurement results, phase calibration was performed whenever the input frequency was changed and was found to be especially important for clock rates higher than 10 GHz.

Figure 14 shows the measured output waveform of the comparator operating at a clock frequency of 18 GHz, with an input frequency of 3 GHz. As can be seen, the differential outputs are fully symmetrical and cross at the waveform mid-points, a consequence of symmetrical layout employed. Operating under this condition, the measured average rise time and fall time of the differential output are 16.9 psec and

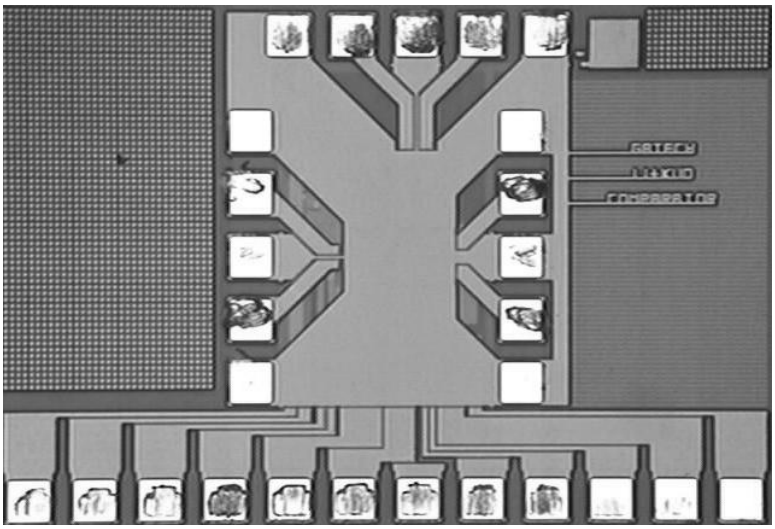

Figure 13: Chip micrograph of the SiGe HBT comparator #1.

16.7 psec (20% to 80%), respectively.

The output waveform of the comparator operating at an even higher frequency (20 GHz clock), with a 5 GHz input, is shown in Figure 15.

The input sensitivity of the comparator, defined to be the minimum differential input peak-to-peak voltage that can be detected, was measured with different clock frequencies and input signal level combinations. The results are shown in Figure 16. With the input signal frequency set at 3 GHz and the sampling rate varied from 9 GHz to 18 GHz, the master-slave comparator shows an input sensitivity ranging from 7.9 mV to 8.9 mV, equivalent to 7.27 bits and 7.10 bits, respectively, for a full input range of 1.2 V peak-to-peak. With the clock frequency at 20 GHz and the input frequency at 5 GHz, the comparator experiences significant resolution degradation, with sensitivity of 40.8 mV, equivalent to 4.9 bits, which is still useful for certain medium-resolution ADCs.

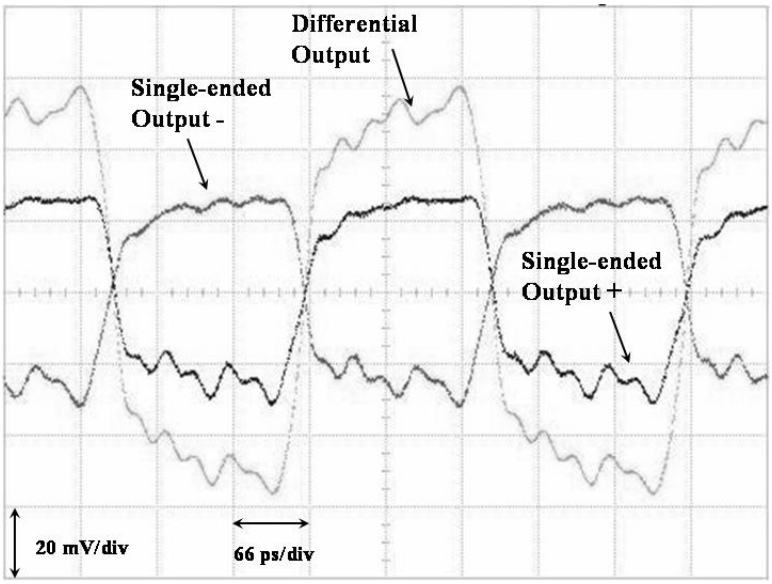

Figure 14: Measured output waveform with an 18 GHz clock and 3 GHz input (20 mV/div in Y axis, 66 psec/div in X axis).

Figure 16 also shows the input sensitivity of the one-stage latch at different sampling frequencies. Better input sensitivity was observed for the master-slave comparator, mainly because of the amplification of the master latch and the reduction in the metastability in the output. The maximum input offset of +/- 4.2 mV was measured with a *dc* input at different sampling rates under 18 GHz. Several different chips were measured and only small variations in our reported results were observed. The measured results of the master-slave comparator are summarized in Table 4.

2.5 Design and Measurement of Comparator #2

The second comparator was implemented with IHP's 200 GHz SiGe HBT technology. The parameters of this fabrication technology are summarized in Table 3. With a 200 GHz f_T/f_{max} HBT technology, the design of comparator #2 has a circuit schematic similar to that of the comparator #1, with some modifications on the latch design and layout to improve the time response of the circuit.

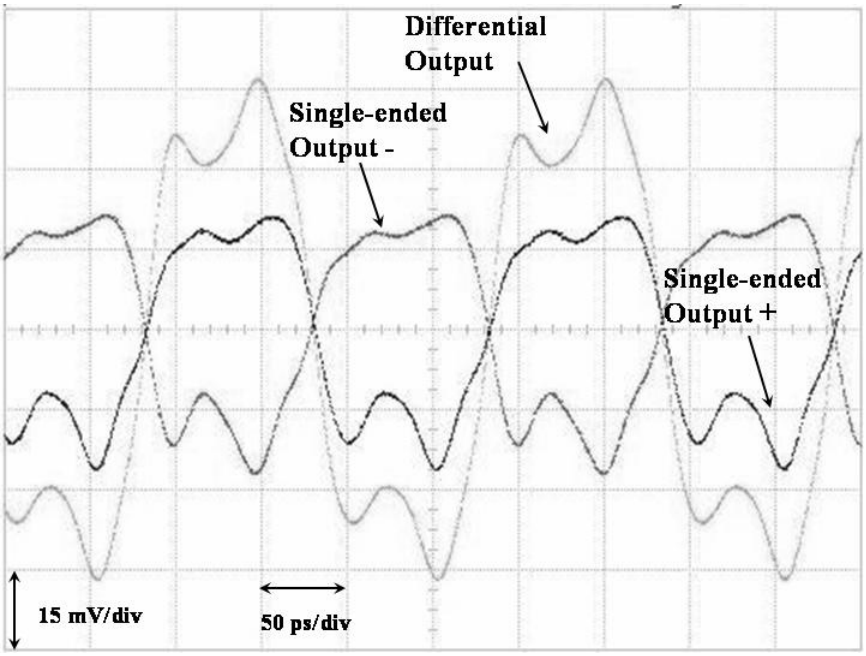

Figure 15: Measured output waveform with a 20 GHz clock and 5 GHz input (15 mV/div in Y axis, 50 psec/div in X axis).

In the new comparator design, to satisfy the high-speed requirement, with the help of transistor's high β, the resistors R_c used to boost the output range of the master latch were removed, and this modification improved the speed of the regeneration. The input buffer also has a high voltage gain to reduce the input-referred offset, as explained in equations (3) and (4).

A very compact and symmetrical layout of the comparator was also achieved in this design, with a core area of only 0.0226 mm^2, about half that of comparator #1.

Table 4: Summary of the Performance of the Comparator #1

Power Supply	+3.5 V
Power Consumption	82 mW
Max. Input Peak-to-Peak Voltage	1.2 V
Rise / Fall Time(20% - 80%)	16.9 psec / 16.7 psec
RMS / PP Jitter	1.17 psec / 5.3 psec
Input Offset	+/- 4.2 mV Max.
Input Sensitivity	8.9 mV @ 18 GHz clock
Sampling Rate	20 GHz Max.

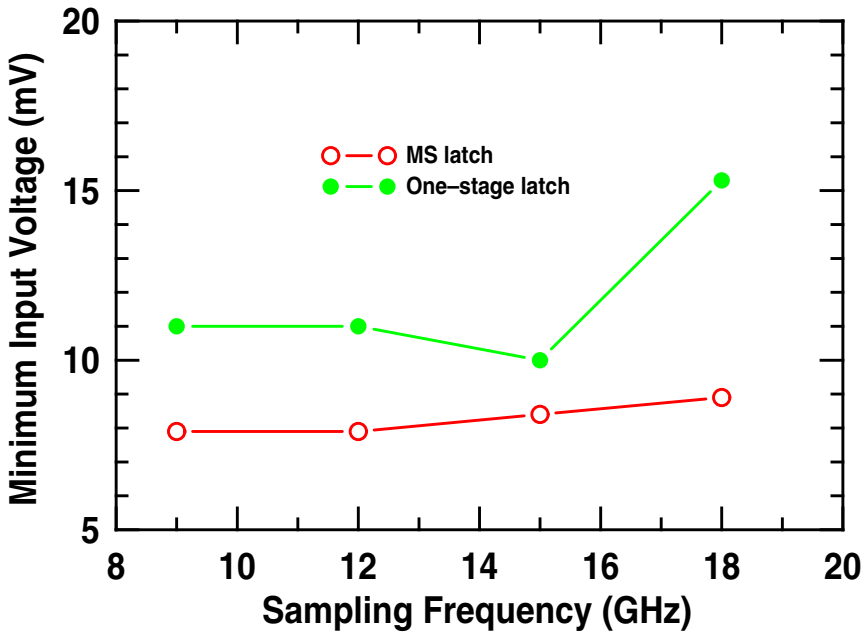

Figure 16: Sensitivity comparison of the master-slave comparator and the one-stage latch as a function of sampling frequency. The input signal frequency is set to 3 GHz.

A proper layout can not only improve the device match, but also reduce the high-frequency parasitics. Large bypass capacitors were used to stabilize the DC current sources and get a better ground.

The chip micrograph of the comparator is shown in Figure 17.

The total die area is 1.731 x 1.141 mm^2 (including bondpads). The large width of the chip is determined by the footprint of the 12 pin dc probes (for current monitoring). The active area of the preamplifier, M/S latches, and output buffer is 0.21 x 0.062 mm^2, and 0.082 x 0.116 mm^2 for the clock buffer. The comparator is characterized on-wafer using 40 GHz probes and cables. Hybrids and baluns are used to convert single-ended signals into differential ones. Phase tuners are used to compensate for different cable phase characteristics before connecting them into the test setup to ensure that the phase of complementary signals are properly maintained since any asymmetry caused by external testing equipments will degrade the performance of the comparator at high frequencies. Operating off a 3.5 V power supply,

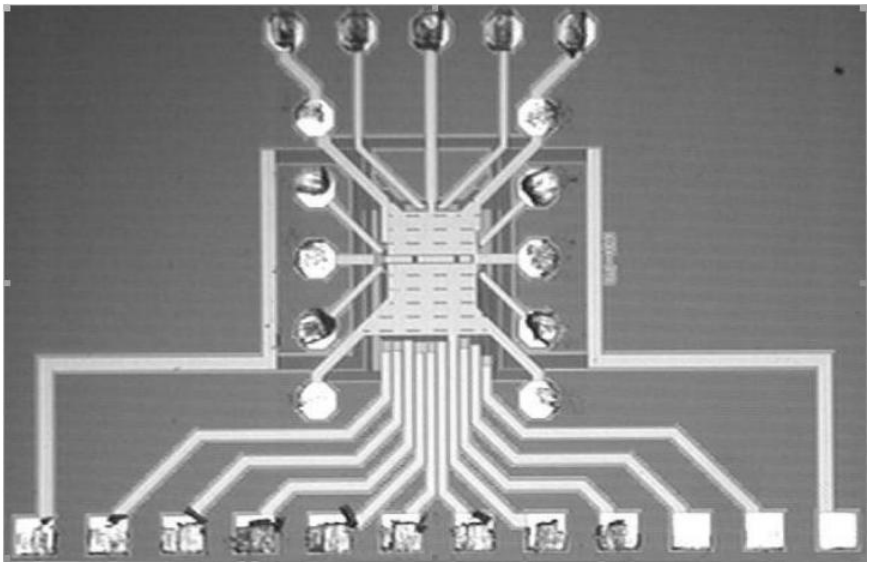

Figure 17: Chip micrograph of the comparator #2 implemented with 200 GHz SiGe HBTs.

the comparator dissipates a total of 405 mW, with the M/S latches consuming 136 mW. The comparator was tested with sine wave input and clock under two different conditions: (1) a 5 GHz input oversampled up to 32 GS/s; and (2) full Nyquist with sampling rates up to 30 GS/s. The output waveforms (both differential and single-ended) of the comparator operating with a 5 GHz input oversampled at 32 GS/s, shown in Figure 18, measured a rise/fall time (20of 12.3/11.2 ps and a random (RMS)/deterministic (peak-to-peak) jitter of 1.15/5.59 ps. The output waveforms of the comparator operating at Nyquist with a sampling rate of 30 GS/s, shown in Figure 19, measured a rise/fall time of 13.0/8.5 ps and a random/deterministic jitter of 1.09/5.80 ps.

The measured input offset voltage of the comparator, caused by device mismatch, as a function of sampling rate with dc input is shown in Figure 20. The offset remains relatively constant at 2.2 mV when sampled below 18 GS/s, reaches a minimum of 1.1 mV at 25 GS/s, and then increases to 16.7 mV at 32 GS/s.

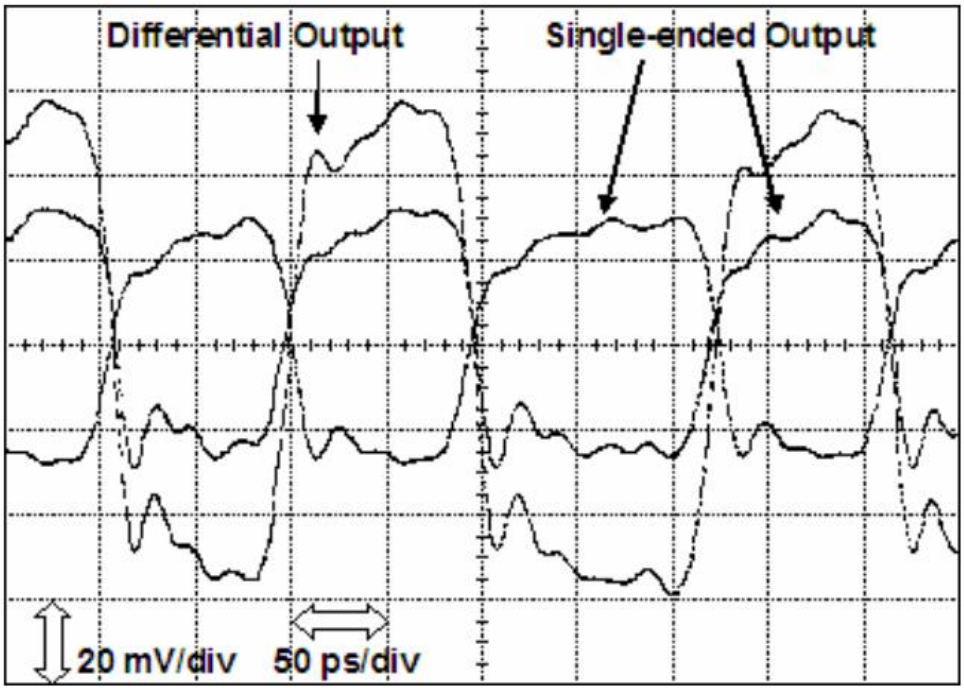

Figure 18: Measured output waveforms of the comparator with a 5 GHz input oversampled at 32 GS/s (20 mV/div, 50 ps/div).

Figure 21 shows the input sensitivity of the comparator, defined as the minimum differential peak-to-peak input voltage that can be detected, as a function of sampling rate operating with a 5 GHz input and at Nyquist. With the 5 GHz input, the measured sensitivity ranges from of 5 mV at 15 GS/s to 37 mV at 32 GS/s, equivalent to 7.9 bits and 5.0 bits of resolution, respectively, for the full input range of 1.2 V peak-to-peak. At Nyquist, the sensitivity ranges from of 12 mV at 20 GS/s to 30 mV at 30 GS/s, equivalent to 6.6 bits and 5.3 bits of resolution, respectively. This demonstrates that the comparator is well-suited for ultra-high-speed medium-resolution oversampled or Nyquist ADCs. The performance of the comparator is summarized in Table 5.

Numerous comparators have been published in the literature, including stand-alone comparators and the ones integrated into complete ADCs. A comparison is

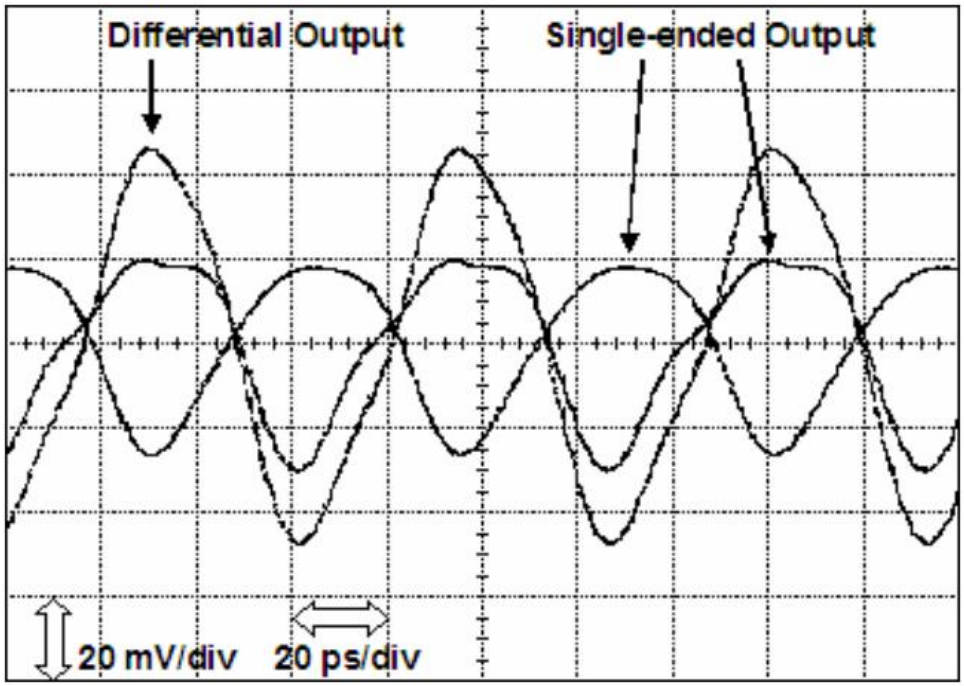

Figure 19: Measured output waveforms of the comparator operating at Nyquist with a sampling rate of 30 GS/s (20 mV/div, 20 ps/div).

made here between the two comparators presented in this thesis and the stand-alone comparators that can be found in the literature. The comparators integrated in the published ADCs are omitted because of the lack of direct measurement results on the comparators themselves. The results are summarized in Table 6.

To our knowledge, the present SiGe comparators achieve the highest resolution to date, together with low power consumption and small core area, when compared with other comparators operating at similar sampling rates. Both comparators can offer significant benefit for the design of ultra-high-speed oversampled or Nyquist ADCs.

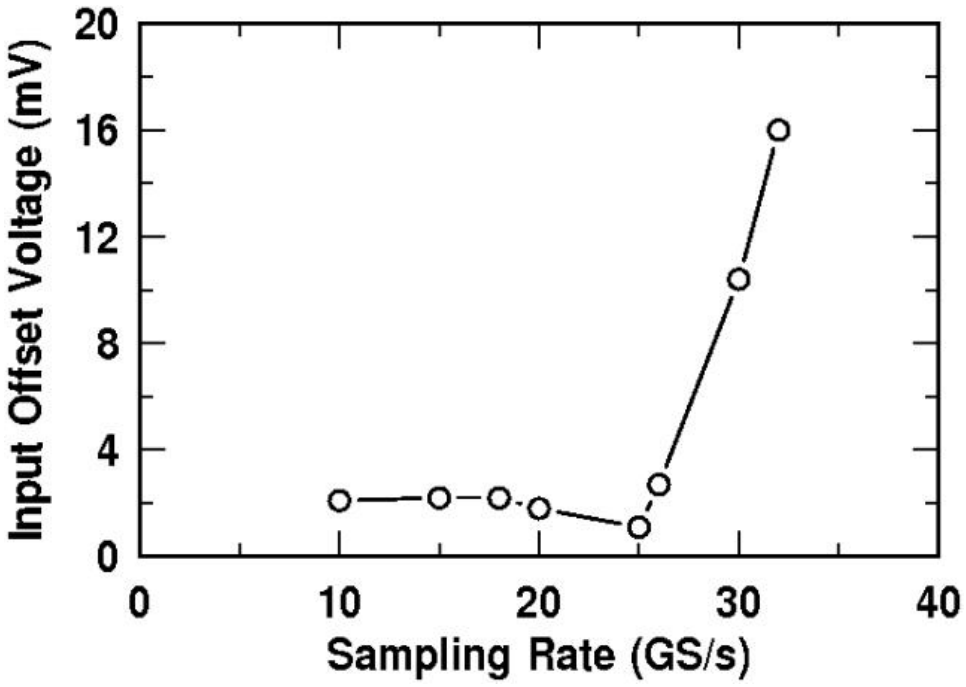

Figure 20: Measured input offset voltage of the comparator as a function of sampling rate.

Table 5: Summary of the Performance of the Comparator #2

Power Supply	+3.5 V
Power Consumption	405 mW
Preamplifier	133 mW
Clock Buffer	90 mW
M/S Latches	136 mW
Output Buffer	46 mW
Rise / Fall Time(20% - 80%)	12.3 / 11.2 psec (in/clk = 5 GHz / 32 GS/s)
Random / Deterministic Jitter	1.09 / 5.80 psec (Nyquist, clk = 30 GS/s)
Input Offset Voltage	$<$ 2.2 mV up to 25 GS/s
Input Sensitivity	8.4 mV (in/clk = 5 GHz / 20 GS/s)
Max. Input Peak-to-Peak Voltage	1.2 V
Sampling Rate	32 GHz Max.

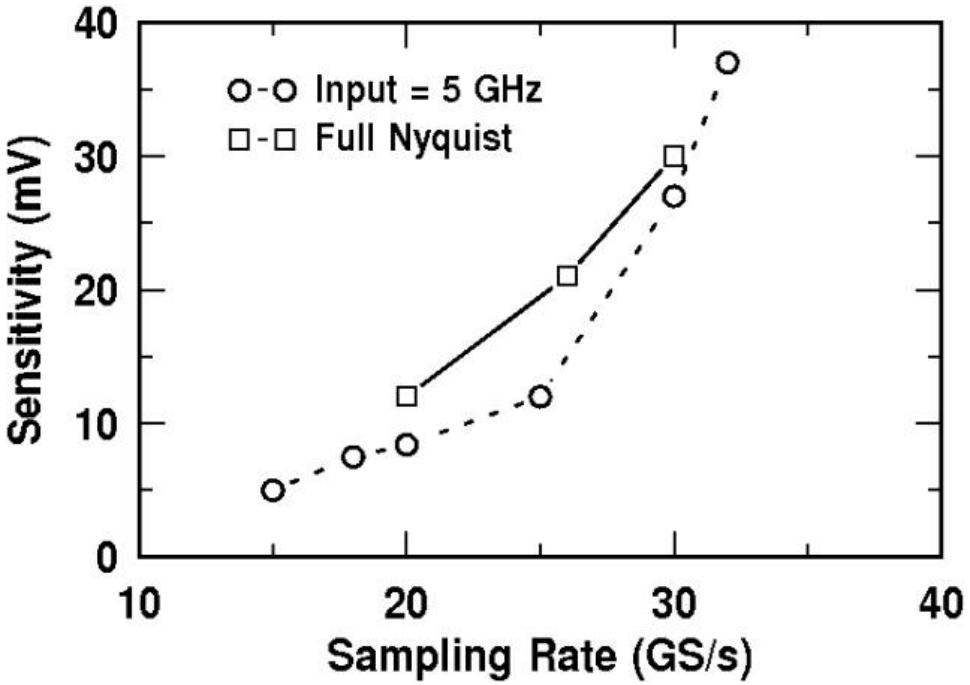

Figure 21: Measured input offset voltage of the comparator as a function of sampling rate.

Table 6: Performance Comparison to State-of-the-Art Comparators Operating in a Similar Frequency Range

Reference	Maximum Sampling Rate [GS/sec]	Sensitivity @ input freq. / sampling rate [mV @ GHz / GS/sec]	Input Offset [mV]	Power Supply [V]	P_{diss} [mW]	Process/f_T [–/GHz]	Active Area [mm^2]
Comparator #1	20	8.9 @ 3 / 18	4.2 Max	+3.5	82 [1]	SiGe/120	0.0455
Comparator #2	32	8.4 @ 5 / 20	2.2 up to 25 GS/sec	+3.5	405	SiGe/200	0.0226
[71]	25	N/A	1.5 typical / 6 Max	+3.3	550	InP / N/A	N/A
[61]	8	30 @ 4 / 8		-6	N/A	GaAs/30	N/A
[62]	5	42 @ - / 5		+1.5/-5	100	GaAs/35	N/A
[63]	5	< 4 @ - / 4		+3	89	SiGe/40	0.0582
[64]	16	N/A		N/A	80	SiGe/55	0.0960
[69]	6	9.2 @ - / 3		+1.5	0.584	0.12 μm CMOS	0.000462
[70]	10	N/A		+1.2	37	0.11 μm CMOS	0.0075

[1]Preamplifier and master/slave latches only

2.6 Summary

Two ultra-high-speed comparators have been designed and fabricated in SiGe HBT technology. Both comparators utilize the ECL configuration and operate off 3.5 V power supplies. The first comparator, implemented with a 0.18 um 120 GHz SiGe HBT BiCMOS technology, can operate at sampling rates of 18 GSamples/s with 7.1 bits of resolution, and 20 GSamples/s with 4.9 bits of resolution. The power consumption for the comparator's core part is 82 mW. The second comparator, implemented with a 200 GHz SiGe HBT technology, can sample a 5 GHz input up to 32 GSamples/s with 5.0 bits of resolution, or sample at Nyquist condition up to 30 GSamples/s, with 7.9 bits of resolution. To our knowledge, the second comparator achieves the best performance combination of sampling rate and resolution when compared with other stand-alone comparators in the literature.

CHAPTER III

TRACK-AND-HOLD AMPLIFIERS

3.1 Introduction

With the rapid evolution of digital CMOS technology, the processing power of modern digital signal processors has greatly improved over time, requiring a large increase in analog-to-digital conversion rates to improve the overall system performance. Therefore, high-speed analog-to-digital converters (ADC) have emerged as a performance-limiting factor in many wireless/wireline systems and measurement instrumentation systems, and are receiving increased attention.

With the increased performance requirements on power, accuracy, and bandwidth, especially from telecommunication and measurement instrumentation systems, the design of ultra-high-speed ADCs represents a serious challenge. The increased bandwidth requirement places great demands on the sampling rate of ADC, while at the same time sufficient ADC accuracy must be maintained, with power consumption being increasingly constrained. To meet the requirements on ADC accuracy, bandwidth, and sampling rate, the design of the track-and-hold amplifier (THA), located in ADC's frond end, is critical, since it will in large measure determine the ADC's overall performance.

In this chapter, two SiGe THAs, operating at 18 GSamples/sec and 40 GSamples/sec, respectively, are presented. The well-known switched emitter-follower (SEF) proposed in [72] is favored in both designs as opposed to the diode-bridge structure [73], because of the low power supply voltage required by an SEF THA. The THA using SEF can operate at very high speed, with good linearity, benefiting from the SiGe HBT's properties of high linearity, low leakage, and high f_T/f_{MAX}.

In both THA designs, an open-loop configuration, without the delay on the feedback loop, is a more suitable choice than the closed-loop structure in order to improve the operational speed.

The first THA presented in this chapter utilizes a conventional SEF design and demonstrates a total harmonic distortion (THD) of -32.3 dBc operating at the rate of 18 GSamples/sec. With its 128 mW power consumption, much lower than most of the other reported high-speed THAs using HBT and operating in giga-samples per second , the presented THA provides an alternative option for the high-speed, low-power ADC design.

The second ultra-high-speed SiGe THA operating at the sampling rate of up to 40 GS/s is also presented in this chapter. Realized with a SEF structure and a fully-differential configuration, this THA employs the feedthrough attenuation network originally proposed in [74] to suppress the signal-dependent non-linear feedthrough interference. A modified version of the SEF design in [75] is used here to alleviate the interference affecting input buffer's operation. A current-compensation circuit is also used in the THA's output buffer to mitigate the current leakage and improve the droop rate.

IBM's 0.18 μm 120 GHz and 0.13 μm 200 GHz SiGe HBT technologies, whose parameters are summarized in Table 2, were used to fabricate THA #1 and #2, respectively.

The design and measurement of the first THA are discussed in section 3.2 and 3.3, respectively. Sections 3.4 and 3.5 describe those of the second THA, followed by a summary in Section 3.6. The content in this chapter was presented at IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) 2005 [76] and IEEE Bipolar/BiCMOS Circuits and Technology 2008 [77].

3.2 Design of THA #1

The block diagram of the THA is shown in Figure 22. The THA has an open-loop

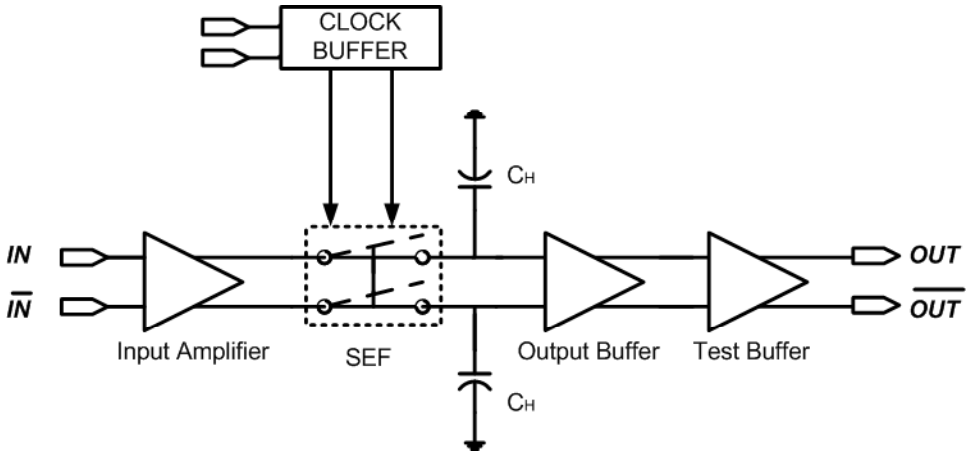

Figure 22: Block diagram of the SiGe HBT THA #1.

architecture to improve its operational speed, and a fully differential configuration is employed to mitigate common-mode noise and suppress the even-order harmonics. The THA consists of a differential input amplifier, SEFs, hold capacitors, and output buffers. Shown in Figures 23 and 24 are the circuit schematics of the THA's input amplifier, SEF, and output buffer.

Wide bandwidth is a basic requirement to guarantee high speed operation of a THA. Simulations show that the poles at the input amplifier's output (at collectors of Q1 and Q2) in Figure 23 and the SEF's output (at emitters of Q9) in Figure 24 have significant impact on the overall bandwidth. When choosing the value of Q1 and Q2's collector resistors R_C, a trade-off has to be made between the bandwidth and the input amplifier's ability to drive the next stage. In addition, the hold capacitors C_H are set to 400 fF to maintain the wide bandwidth while mitigating the loss of the droop rate. All switching HBTs (Q7, Q8, Q9, Q10, Q11, and Q12) are biased at the peak f_T current density. Moreover, the emitter size of Q9 and Q10 should be small

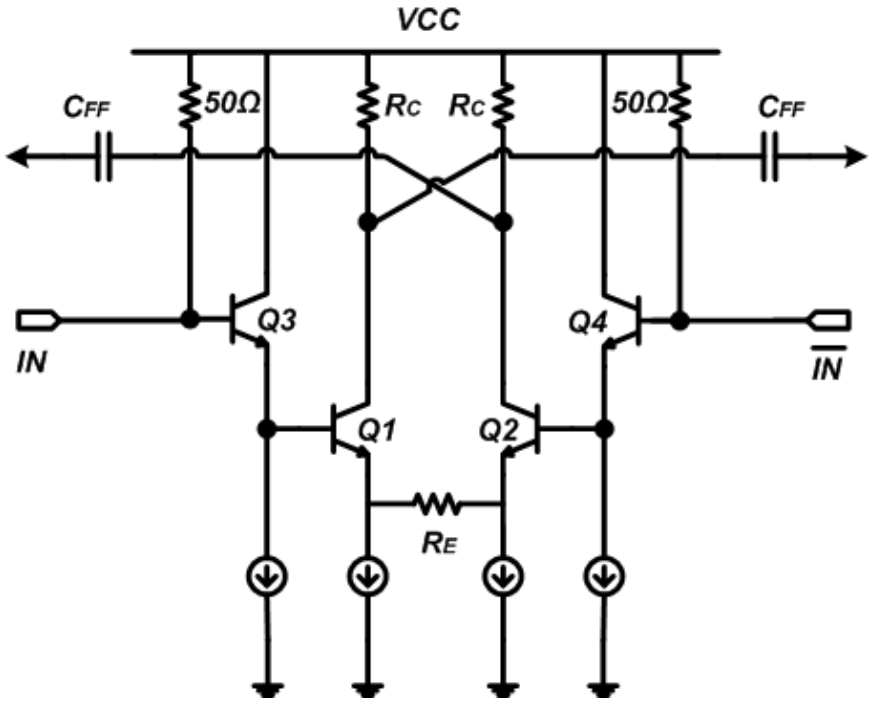

Figure 23: The schematic of the THA #1's input amplifier.

to minimize the hold-mode feedthrough and to speed up the switching operation.

In the hold mode, the non-linear emitter-base junction capacitance of the bipolar transistor (Q9 in Figure 24) in the SEF will cause the feedthrough interference coupled from the input amplifier and worsen the pedestal error. The ratio of the feedthrough and the signal can be expressed as follows:

$$A_{feedthrough} = \frac{C_{BE,Q9}}{C_H + C_{BE,Q9}}. \tag{10}$$

The introduction of capacitors C_{FF} shown in Figure 24 can compensate the feedthrough in some degree, by injecting the charge dump opposite to that coupled from the emitter-base junction capacitors into the hold capacitors. As a result, the feedthrough with a compensation can be expressed [72]:

$$A_{feedthrough} = \frac{C_{BE,Q9}}{C_H + C_{BE,Q9}}(1 - \frac{C_{FF}}{C_{BE,Q9}}). \tag{11}$$

If C_{FF} can be chosen to approximate $C_{BE,Q9}$, the feedthrough will be largely suppressed. However, the compensation could be limited since the BE junction capacitors

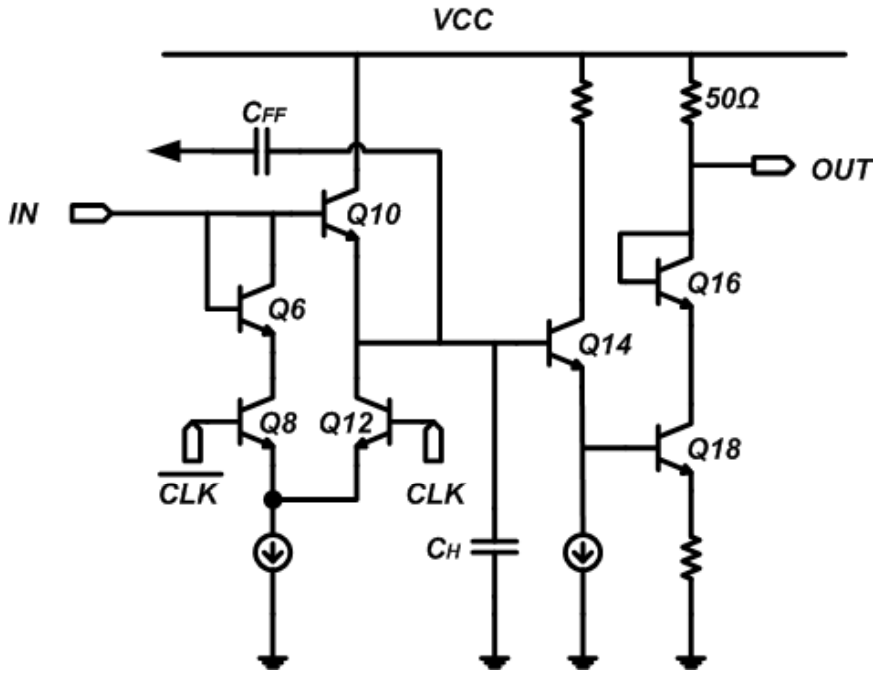

Figure 24: The simplified schematic of THA #1's SEF and output buffer.

are non-linear and varying with the input signal.

The compensation capacitors C_{FF} shown in Figure 24 are implemented as illustrated in Figure 25.

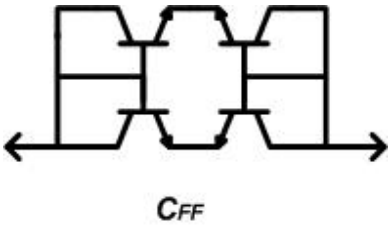

Figure 25: Compensation capacitor C_{FF}.

Linearity is one of the critical THA parameters and is directly related to the THA's dynamic range and total harmonic distortion (THD). It can be simply estimated using periodic steady state (PSS) analysis. Figure 26 shows the PSS simulation results on the THA's output power of the fundamental tone and the third-order harmonic. The

input 1-dB compression point is around 0 dBm. If it is assumed that the third-order harmonic is dominant in the THD, then the simulated spurious-free dynamic range (SFDR) when the input is 1.0 Vpp, is around 35 dBc.

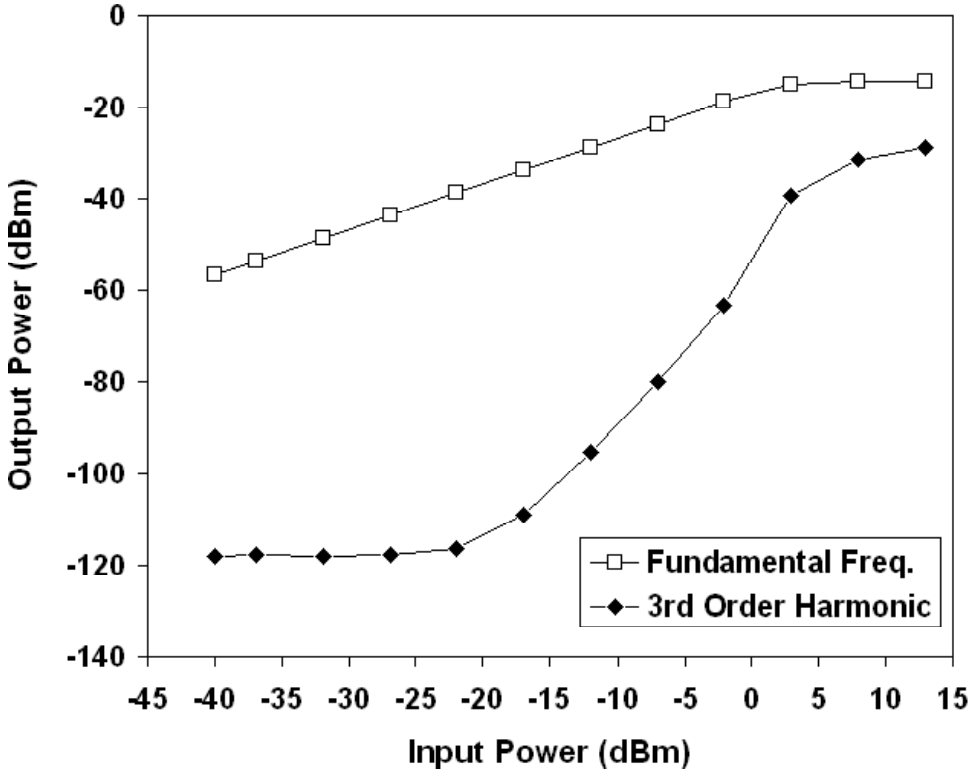

Figure 26: Simulated THA output power of the third-order harmonic and fundamental frequency, with an 18 GS/sec sampling rate and 2 GHz input.

Aperture jitter, defined as the random variation in the aperture time from sample-to-sample, is a limiting factor that affects THA accuracy, and is a function of temperature variation, the input signal's magnitude and instantaneous slope, and other random sources [19]. Aperture jitter sets an upper limit on the maximum input signal frequency that can be sampled by a THA with a specified accuracy. It can be shown that for a full-scale sinusoidal signal with a frequency f, to obtain an n-bit accuracy

on the THA, the following relation must be satisfied

$$f < \frac{1}{2\pi \times 2^n \times t_{aj}}, \tag{12}$$

where t_{aj} is the aperture jitter specified as an RMS value [78]. Minimizing the clock signal's rise/fall time is desired due to its significant contributions to the aperture jitter. In this work, a stand-alone clock buffer translating a sinusoidal signal to a square wave clock signal was fabricated separately, and its schematic is shown in Figure 27.

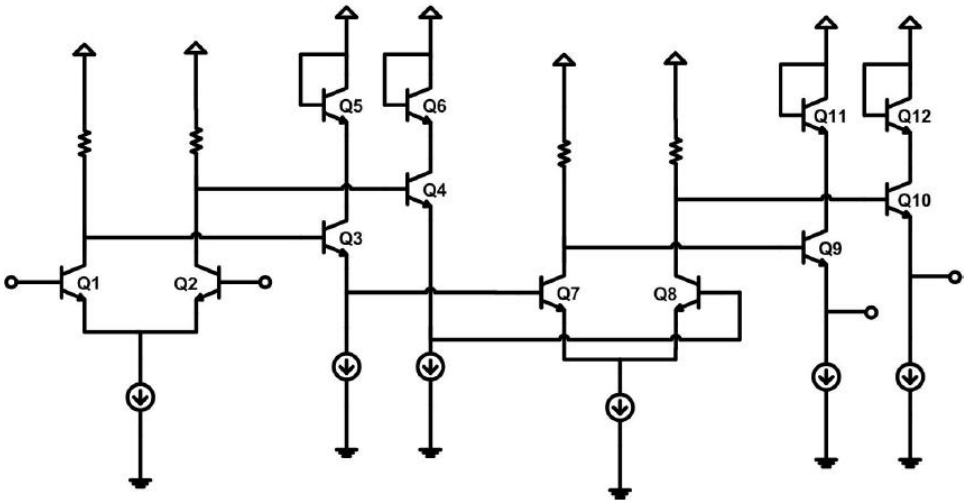

Figure 27: The schematic of a clock buffer used to drive the THA.

Measurements on this chip show that with an 18 GHz sinusoidal signal applied on the input, an 18 GHz square wave was observed in the output with a 1.2 psec RMS jitter. With the assumption that the clock jitter is the dominant source for the aperture jitter, and ignoring other contributions [79], the maximum input signal frequency for a 5-bit accuracy THA from (12) is 4.14 GHz.

3.3 Layout and Measurements of THA #1

For circuits working in the frequency range of tens of GHz, inappropriate circuit layout can cause significant performance loss. The THA employs a fully differential configuration to suppress the even-order harmonics and minimize the effects of common-mode noise, and therefore a strictly symmetrical layout is essential to maintain the advantage of the fully differential structure. Moreover, parasitics are inevitably introduced during layout and will degrade the circuit's high-speed operation. Special care has to be taken to minimize their impact.

To this end, interconnects in the critical path are kept short to reduce layout parasitics. As a result of this, the THA core (input amplifier + SEFs + output buffers) was made extremely compact and occupies an area of only 120×200 μm^2. The crossing area between different metal layers was kept small to reduce crossing capacitance without increasing series resistance. Instead of 90° turns in the signal paths, 45° tapered lines were used to minimize internal reflections. On-chip by-pass MIM capacitors were connected to the *dc* supply lines and current mirrors for high-frequency decoupling. A robust ground is formed by using the top copper metal covering all sub-blocks. Twelve *dc* supply lines were used to monitor the *dc* bias of critical points in the circuit and allow options for tuning the circuit if required.

The overall die size, including bondpads, is 1.58×1.7 mm^2, and the chip micrograph is shown in Figure 28. On-wafer measurements of the THA were performed using 40 GHz probes and cables. Hybrids were used to split the single-ended input signals into differential signals. Since any test-setup-induced mismatch in the differential clock input can cause severe performance degradation, phase tuners were used to adjust the phase of the cables to exactly 180° phase difference after passing through the hybrid. The test setup for measuring the THA is shown in Figure 29.

Figure 30 shows the measured differential output waveform of the THA operating at a sampling rate of 16 GS/sec, with an input frequency of 2 GHz. The output

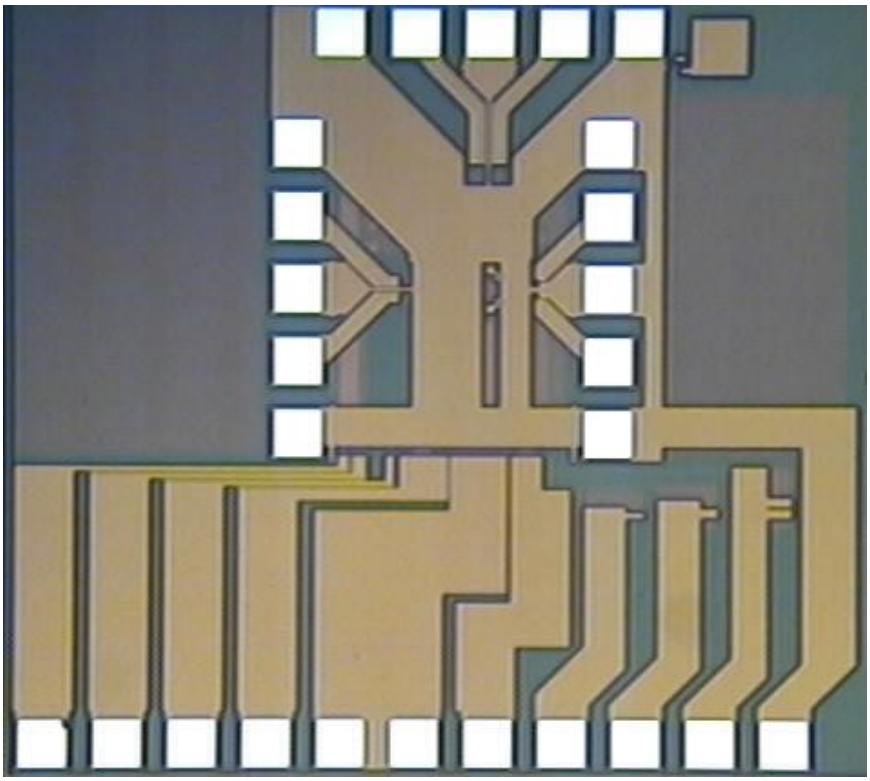

Figure 28: Chip micrograph of the SiGe THA.

spectrum with an 18 GS/sec sampling rate and 2 GHz input frequency is shown in Figure 31. It can be seen from this figure that the second harmonic is significantly suppressed, which is a direct consequence of the fully differential design and symmetrical layout employed in the design. The measured THD is -32.3 dBc, equivalent to a 5.1-bit resolution, under these measurement conditions. Figure 32 shows the measured output harmonic distortions as a function of sampling rate with a 2 GHz input signal. The measured results of this SiGe THA, applied with a 2 GHz input signal, are summarized in Table 7.

A comparison is made between the THA presented in this work with other THAs (both SiGe and III-V) that can be found in the literature. The results are summarized in Table 8. It can be seen that the present SiGe THA operates at the highest clock

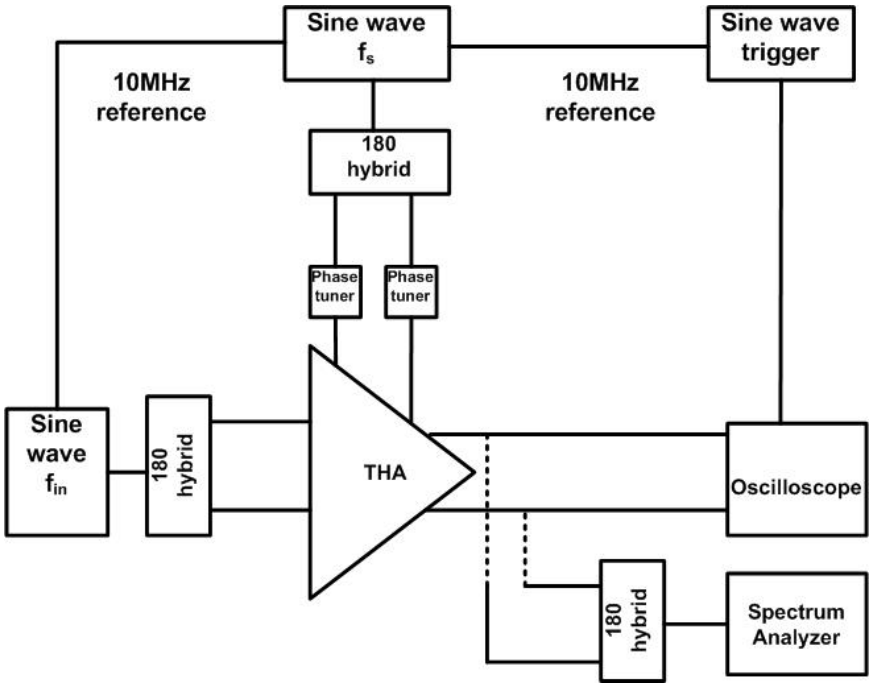

Figure 29: The test setup for measuring THA.

rate under medium resolution while consuming the second to least power.

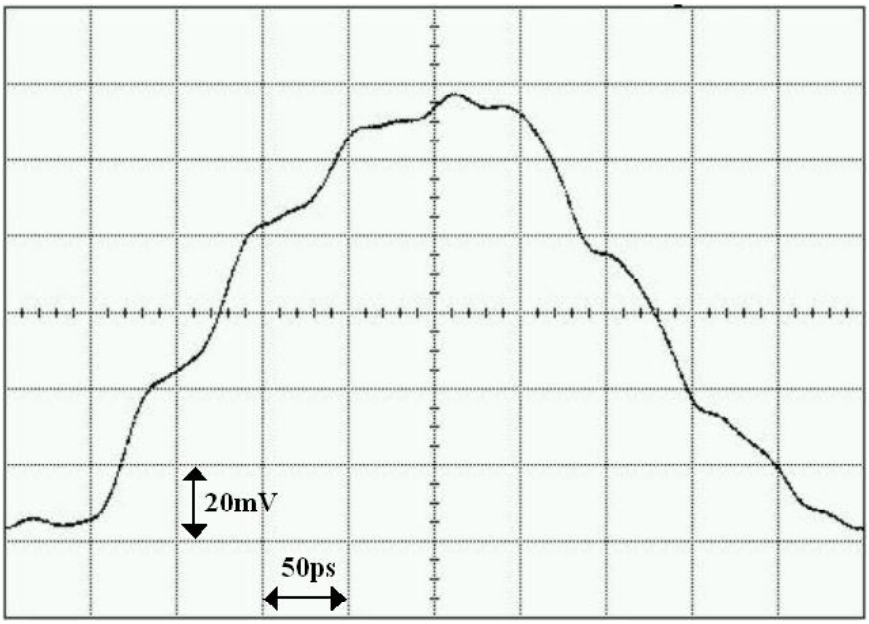

Figure 30: Measured differential output with a 16 GS/sec sampling rate and 2 GHz 1.0 Vpp input.

Table 7: Summary of the SiGe THA's Measured Performance.

Power Supply	+3.5 V
Power Consumption(Clock Excluded)	128 mW
Input Peak-to-Peak Voltage	1.0 V
Bandwidth in Track Mode	7 GHz
Differential Droop Rate	$<$ 10 mV/nsec
Pedestal Error	$<$ 10 mV
THD@18 GS/sec f_{sample}, 2 GHz f_{in}	-32.3 dBc
Max. Sampling Rate	18 GS/sec

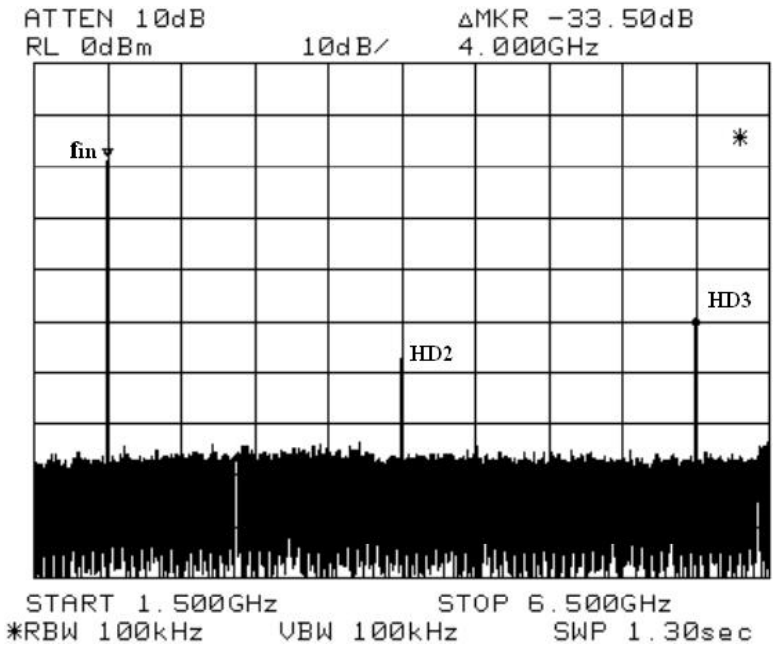

Figure 31: Measured output spectrum with an 18 GS/sec sampling rate and 2 GHz 1.0 Vpp input.

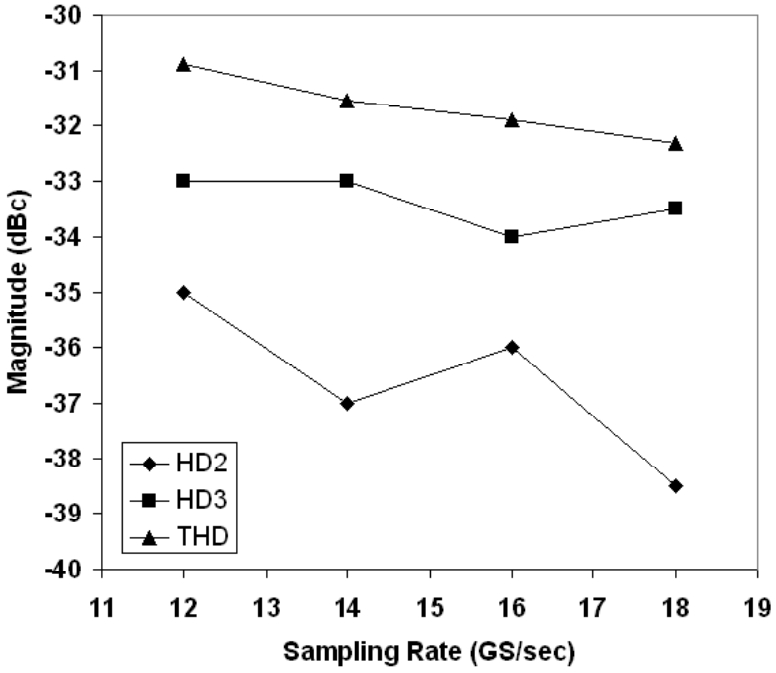

Figure 32: Measured output harmonic distortions as a function of sampling rate with a 2 GHz input signal.

Table 8: Performance Comparison to State-of-the-Art THAs Operating in a Similar Frequency Range

Reference	f_{sample} [GS/sec]	f_{in} [GHz]	Measured THD [dBc]	Bandwidth [GHz]	Input [Vpp]	Power Supply [V]	P_{diss} [mW]	Process/f_T [–/GHz]
This work	18	2	-32.3	7	1.0	+3.5	128	SiGe/120
[19]	10	10	-30	16	0.6	-3.7	-	SiGe/120
[80]	12.001	12	-23.3	> 14	1.0	-5.2	390	InP/120
[81]	12.1	1.5	-52.4	5.5	1.0	+3.5	700	SiGe/200
[73]	4	8	-30	10	0.6	+5.2	550	SiGe/45
[82]	2	0.9	-54	0.9	0.8	-3.3	550	SiGe/65
[83]	10	1	-29.5[1]	2.7	1.0	+3.3	30[2]	SiGe/200

[1]Measurement on single-ended output.
[2]THA core power consumption.

3.4 Design of THA #2

Some high-speed THAs with a different operational range and linearity performance have been reported recently. For instance, a SiGe THA with an improved version of pseudo-differential structure, inspired by the design in [84], was reported in [81]. It achieves -52.4 dBc of total harmonic distortion (THD) at the rate of 12.1 GS/s, and is the fastest 8-bit Si-based THA achieved to date. A 40 GS/s SiGe THA with a switched-emitter-follower (SEF) configuration and a low-noise input preamplifier was reported in [85], and [86] employed a 3-stage SEF architecture to realize a distributed SiGe THA that achieves the fastest sampling rate demonstrated to date, 50 GS/s.

The traditional THA with a SEF configuration [72] has some drawbacks that affect the operation of the THA and degrade performance. One major limitation is the hold-mode feedthrough interference that causes large pedestal error in the voltages of hold capacitors. This problem comes from the signal coupling from the input amplifier through the non-linear emitter-base junction capacitance of the bipolar transistor in the SEF. To suppress this feedthrough interference, a feedthrough attenuation network is introduced in the present THA, and the block diagram is shown in Figure 33.

In the track mode, the feedthrough attenuation network does not function, as switch 1 is open. In the hold mode, however, switch 1 is closed and the output of the feedthrough attenuation network will be approximately out of phase with respect to that of the input buffer. As a result, the combined signal will be largely attenuated during the hold mode. The whole system employs a fully-differential configuration to mitigate common-mode noise and suppress even-order harmonics.

The simplified schematic of the input buffer and feedthrough attenuation network is shown in Figure 34. To achieve high linearity in the input buffer, emitter-degenerated differential pairs are used in the design of input buffer, with two transistors ($Q5$ and $Q6$) added to suppress the non-linearity caused by V_{BE} modulation.

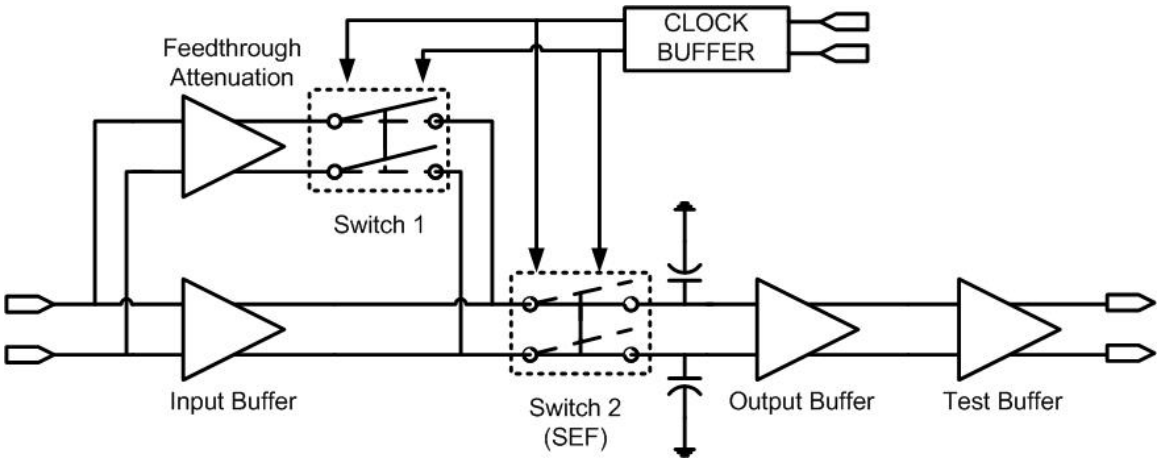

Figure 33: The THA block diagram.

The schematic of the SEF is shown in Figure 35. Compared with the conventional SEF design presented in [72], a resistor R_h and a transistor $Q14$ are added in this SEF. By introducing an additional emitter-follower stage, the base voltage of $Q13$ will be clamped into a certain range instead of experiencing large voltage variations during the track and hold transition period and pushing the input buffer's differential pair into saturation during hold mode. The base voltage of $Q14$, acting as the main switch, will be down by a value of $-I_h{*}R_h$ in the track to hold-mode transition, and turning $Q14$ off.

The design of the output and test buffer is shown in Figure 36. Current compensation is provided to reduce the current leakage from the hold capacitors and hence decrease the droop rate. Simulations show that the average current leakage is reduced by 60 percent to the value of 12 nA.

3.5 Measurement Results

The layout of the SiGe THA is strictly symmetrical to fully leverage the differential configuration. The THA chip has a die size of 1.8×1.0 mm^2 including bondpads and is shown in Figure 37. On-wafer measurements of the THA were performed using 40

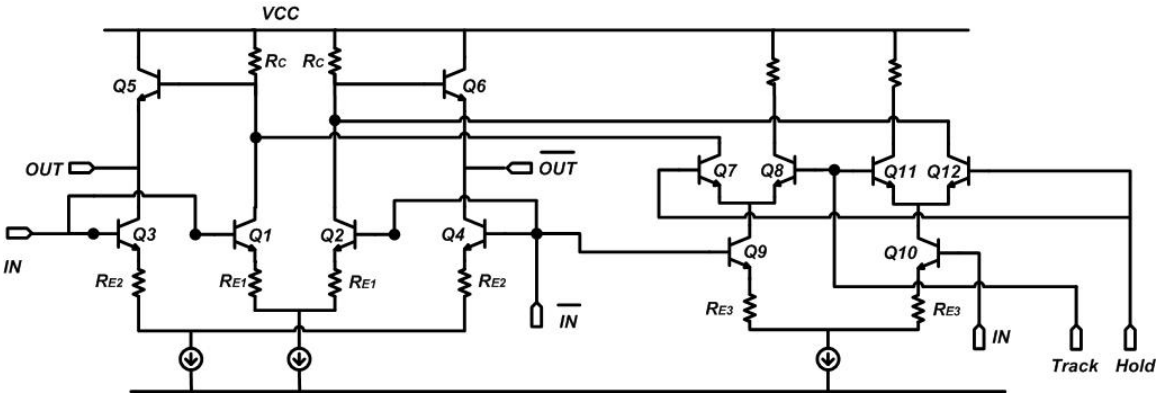

Figure 34: Simplified schematic of the input buffer and feedthrough attenuation network.

GHz probes and cables. Hybrids were used to split the single-ended input signals into differential signals. A wideband oscilloscope, a spectrum analyzer, a PNA network analyzer, and two 50-GHz signal generators were used in the measurements.

Figure 38 shows two measured single-ended output waveforms of the THA operating at the sampling rate of 40 GS/s, with a 6 GHz input frequency, and Figure 39 shows the combined waveforms of these two single-ended signals.

The output spectrum with a sampling rate of 40 GS/s and a 10 GHz input frequency is shown in Figure 40. It can be seen from this figure that the second-order harmonic distortion is suppressed, which is a direct consequence of the fully differential design and symmetrical layout employed in the design. The measured THD is -32.4 dBc under these measurement conditions. The THD improves to -44.2 dBc when the sampling rate is 18 GS/s and the input signal frequency is 3 GHz, and to -50.5 dBc under the condition of 12 GS/s and 2 GHz input signal. The THA's measured S-parameters in the track mode are illustrated in Figure 41, 42, 43, 44, respectively.

Performed in a single-ended configuration, the measurement shows that the S21 is around -9 dB in the passband, including the signal loss from the single-ended

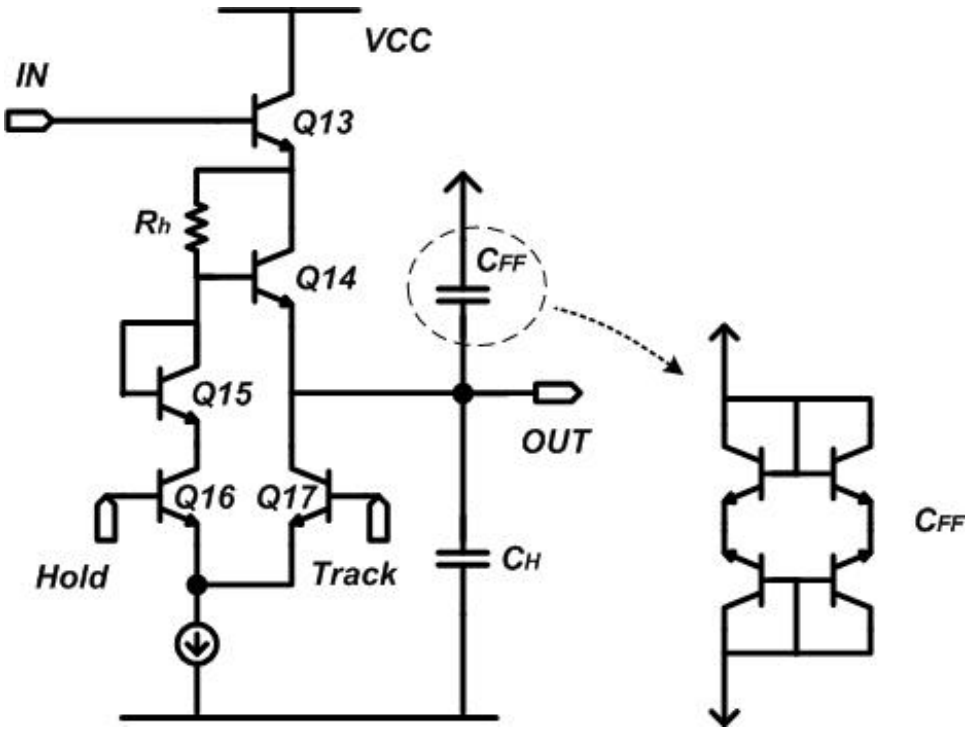

Figure 35: Schematic of the THA's SEF.

configuration. The 3-dB bandwidth is tested to be around 16 GHz in the track mode. A two-tone test result is also shown in Figure 45, with an input power set to -4 dBm. Denoted as $\triangle P$, the difference between the third-order intermodulation product in output and the desired output power in the fundamental, is around 39.2 dB. The third-order input intercept point (IIP3) can then be calculated from these data obtained from the two-tone test, through the following equation:

$$IIP3 = P_{in} + \frac{\triangle P}{2}, \tag{13}$$

where P_{in} is the input power of the fundamental in dBm. The IIP3 is therefore 15.6 dBm at the 10 GHz input frequency. The measured results of this SiGe THA are summarized in Table 9.

A comparison has also been made between our SiGe THA and other THAs that can be found in the literature. The results are summarized in Table 10. It can be seen that the present SiGe THA has a wide operational range, with comparable

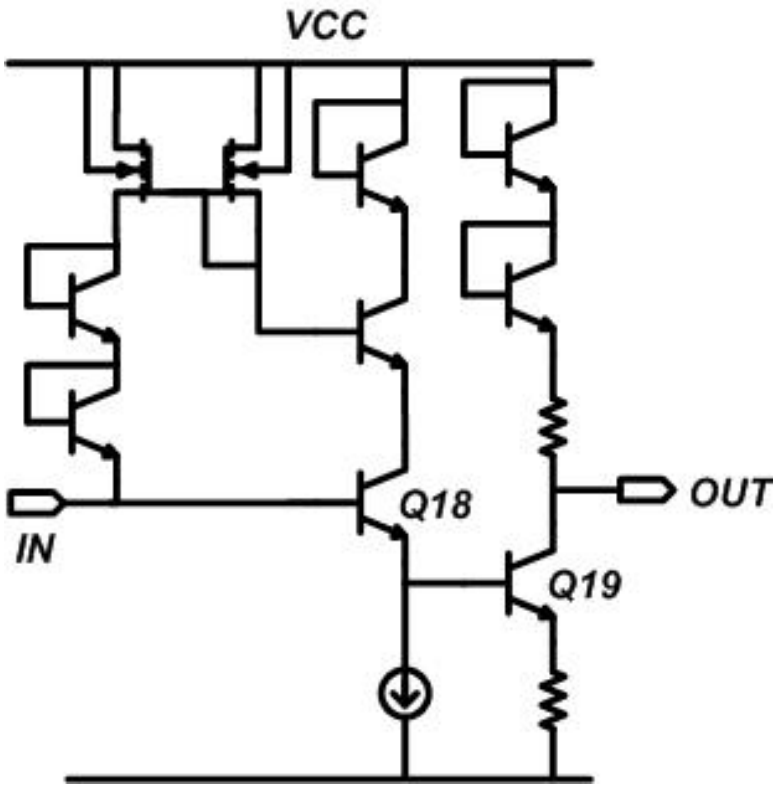

Figure 36: Schematic of THA's output and test buffer.

characteristics to other THAs operating in different conditions. Compared with the THAs published in literature with the operational range from 10 GS/s to 20 GS/s, the present THA demonstrates a THD comparable to the best one achieved to date to our knowledge in Si technology, reported in [81], with much improved high-frequency characteristics. On the other hand, in the operational range of 30 GS/s and above, the present SiGe THA still exhibits robust characteristics compared to the fastest THAs in terms of linearity, power consumption, and sampling rate.

3.6 Summary

Two ultra-high-speed SiGe THAs with a fully differential configuration are reported. This first SiGe THA can operate at an 18 GS/sec sampling rate with -32.3 dBc of THD, and consumes only 128 mW of power with a die area of only 1.58 × 1.7 mm^2. The second SiGe THA can operate at a 40 GS/s sampling rate with -32.4 dBc

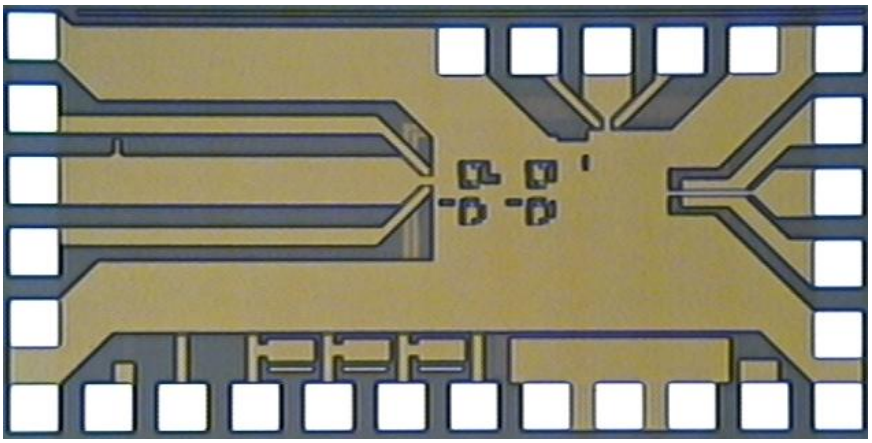

Figure 37: Chip micrograph of the SiGe THA.

Table 9: Summary of the SiGe THA's Measured Performance.

Power Supply	+5.5 V
Power Consumption (Clock Excluded)	560 mW
Input Peak-to-Peak Voltage	1.0 V
Bandwidth in Track Mode	16 GHz
Differential Droop Rate	$<$ 10 mV/nsec
THD@40 GS/sec f_{sample}, 10 GHz f_{in}	-32.4 dBc
@18 GS/sec f_{sample}, 3 GHz f_{in}	-44.2 dBc
@12 GS/sec f_{sample}, 2 GHz f_{in}	-50.5 dBc
Max. Sampling Rate	40 GS/sec

of THD, and consumes 560 mW of power with a core area of 0.83×0.22 mm^2.

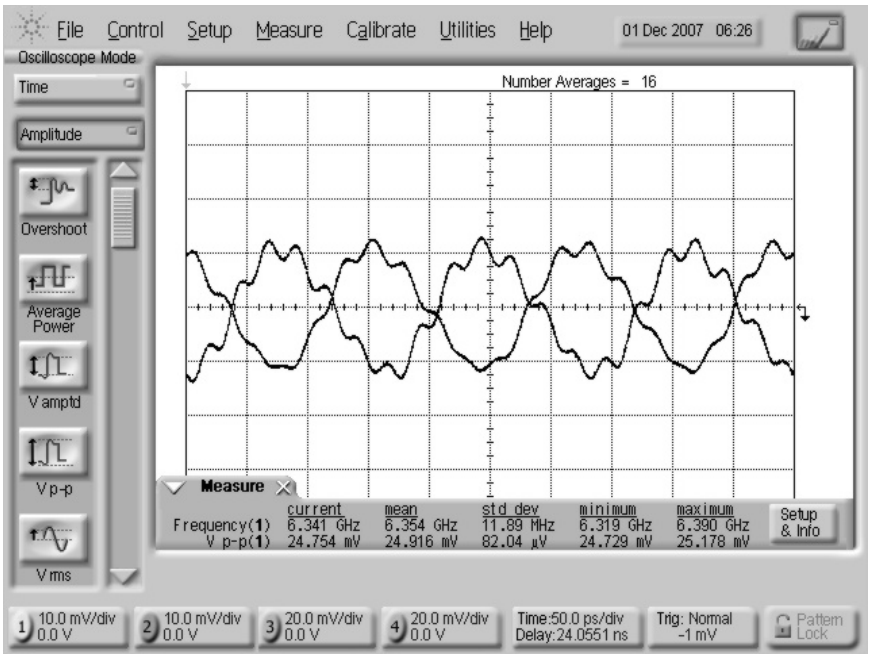

Figure 38: Measured two single-ended outputs with a 40 GS/s sampling rate and a 6 GHz 1.0 Vpp input.

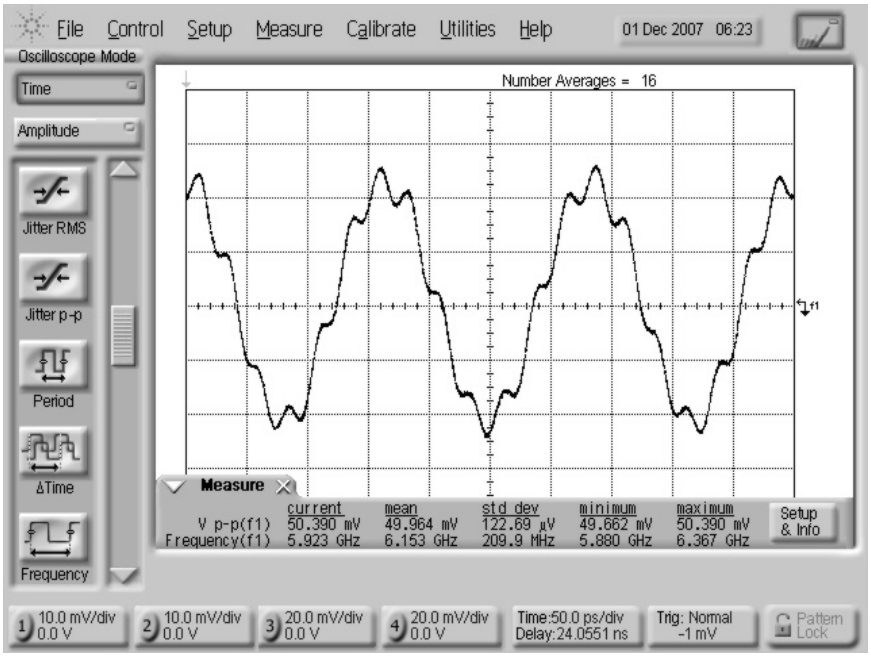

Figure 39: Combined waveform of these two differential outputs shown in Figure 38.

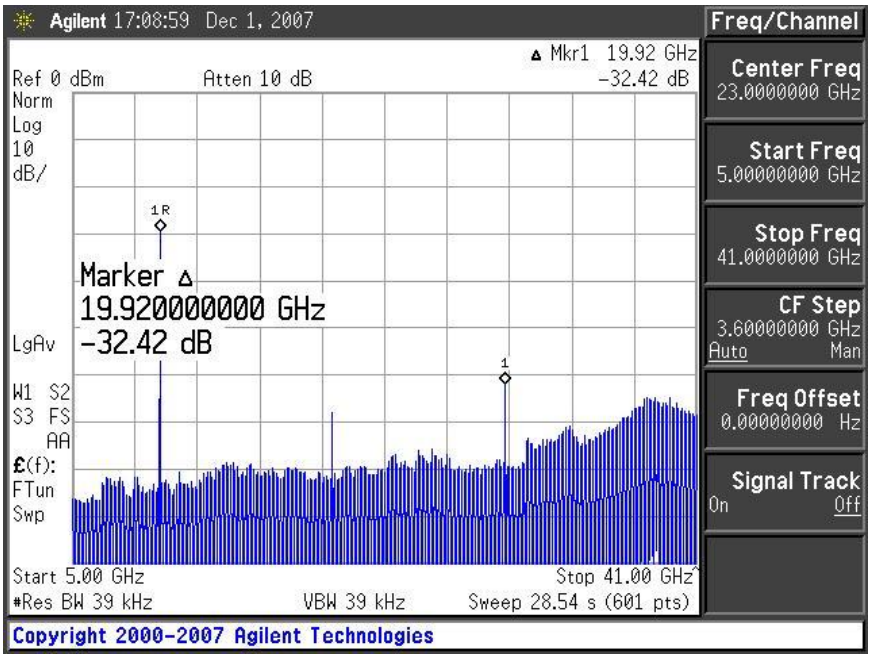

Figure 40: Measured output spectrum with a sampling rate of 40 GS/s and a 10 GHz 1.0 Vpp input.

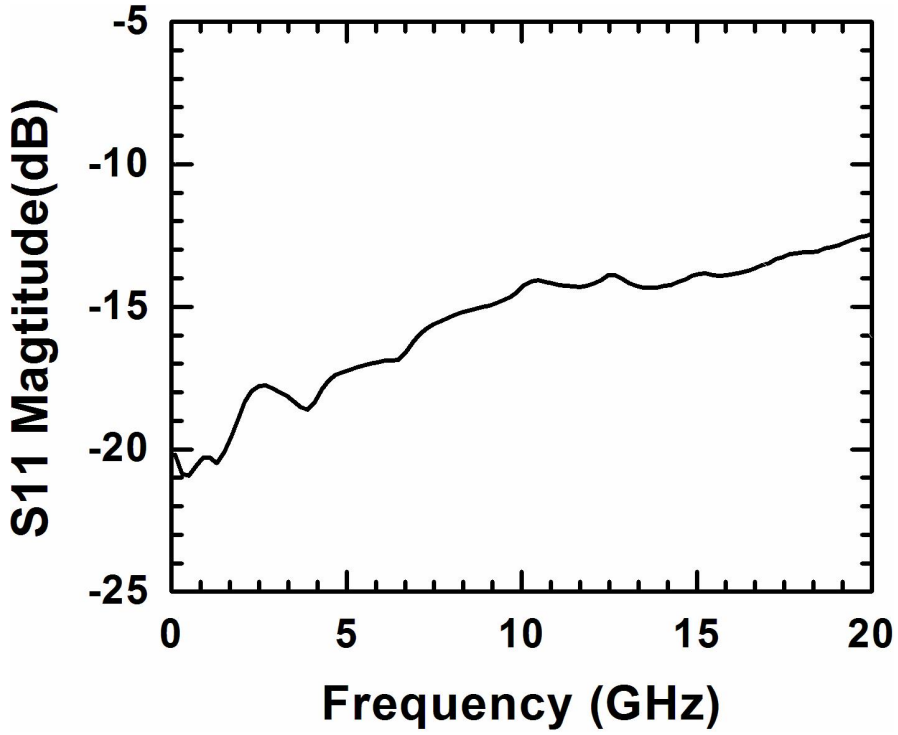

Figure 41: Measured THA's S11 in the track mode.

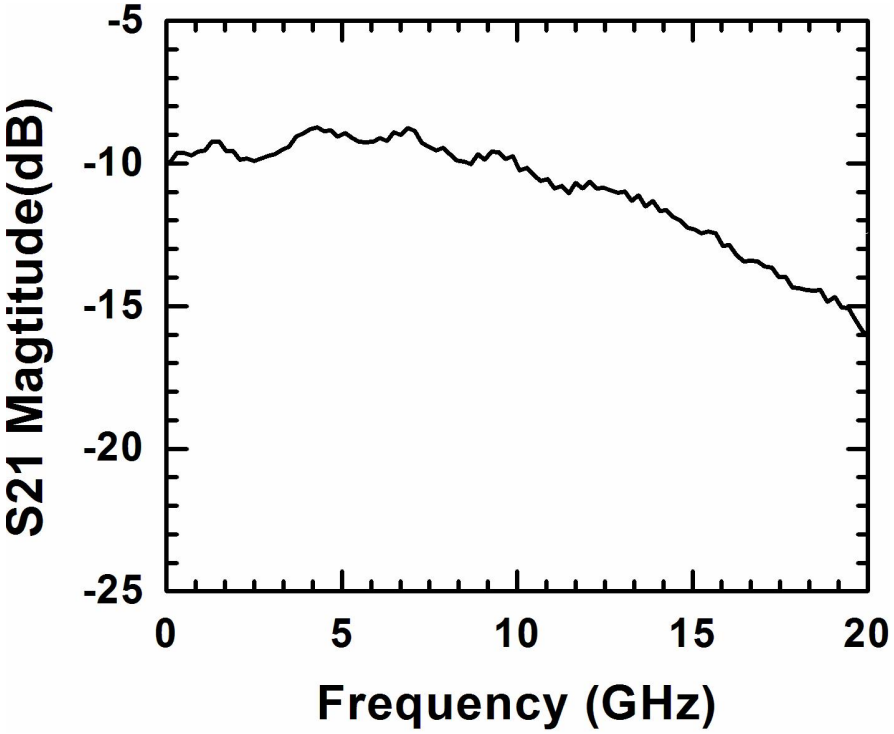

Figure 42: Measured THA's S21 in the track mode.

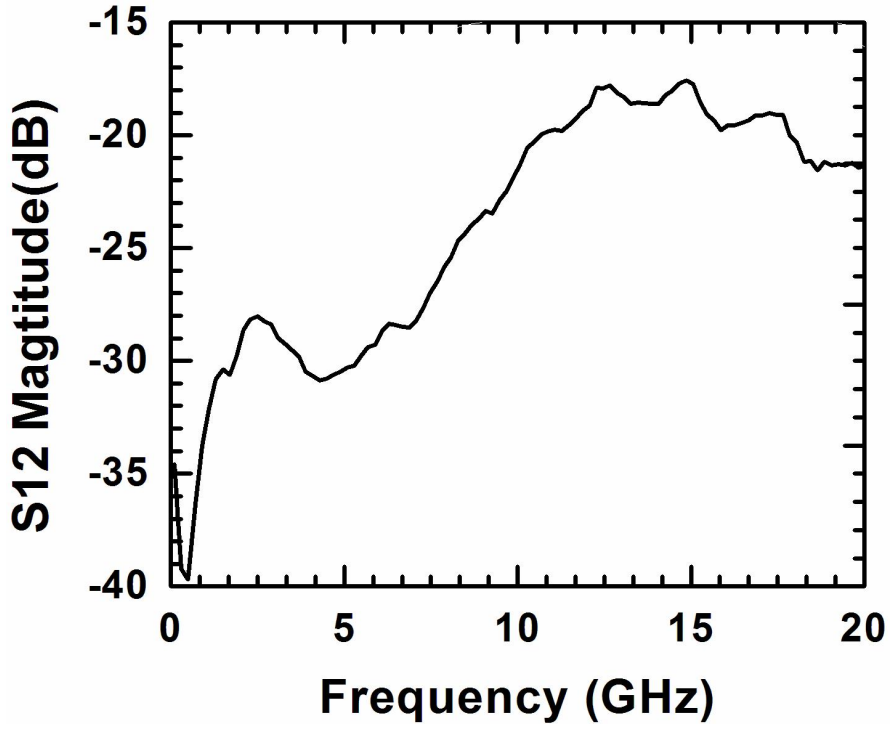

Figure 43: Measured THA's S12 in the track mode.

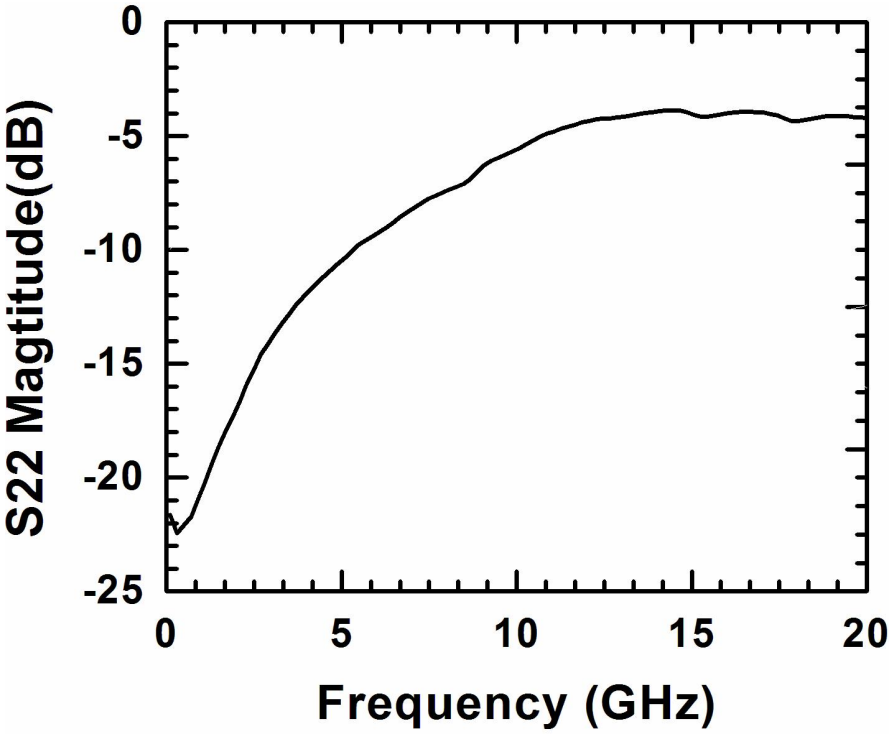

Figure 44: Measured THA's S22 in the track mode.

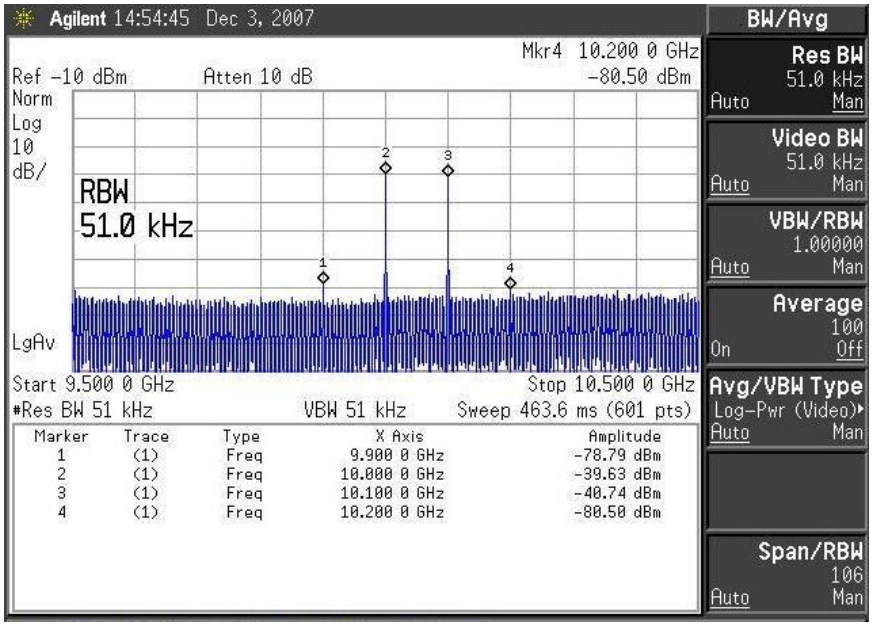

Figure 45: Two-tone test at 10 GHz, with an input power of -4 dBm.

Table 10: Performance Comparison to State-of-the-art THAs Operating in a Similar Frequency Range

Reference	Max. f_{sample} [GS/sec]	THD@f_{in}/f_{sample} [dBc @ GHz / GS/s]	Bandwidth [GHz]	Input	Power Supply [V]	P_{diss} [mW]	Process/f_T [–/GHz]
This work	40	-32.4 @ 10/40 -44.2 @ 3/18 -50.5 @ 2/12	16	1.0 Vpp	+5.5	560	SiGe/200
[81]	12.5	-52.4 @ 1.5/12.1 -49.5 @ 3.0/12.5	5.5	1.0 Vpp	+3.5	700	SiGe/200
[85]	40	-29 @ 10/40 -27 @ 19/40	43	-	+3.6	540	SiGe/160
[86]	50	-35 @ 40.001/40[1]	42	0 dBm	+4, +3	640	0.18-μm SiGe BiCMOS
[80]	12.001	-23.3 @ 12.001/12[1]	> 14	1.0 Vpp	-5.2	390	InP/120
[87]	30	-29 @ 7/30	7	-12 dBm	+1.8	270	0.13-μm CMOS
[76]	18	-32.3@ 2/18	7	1.0 Vpp	+3.5	128	SiGe/120
[73]	4	-30 @ 8/4	10	0.6 Vpp	+5.2	550	SiGe/45

[3]Measured results from the beat frequency test.

CHAPTER IV

LOW-PASS ANALOG-TO-DIGITAL ΣΔ MODULATOR

This chapter will present the design of a high-speed second-order, low-pass AD ΣΔ modulator using SiGe HBT technology, and will cover: 1) characterization of ADC; 2) theoretical fundamentals of ΣΔ ADC; 3) design methodology of specific building blocks and system; and 4)simulation and measurement on the circuits.

4.1 Characterization of ADC

As discussed in Chapter one, ADCs can be classified into two categories based on the sampling methods: Nyquist ADC and oversampling ADC. A brief discussion on the sampling theory is presented in this section followed by a more detailed exploration on the ΣΔ ADC.

4.1.1 Nyquist Sampling and Quantization

In the sampling process, when a continuous-time signal $x(t)$ is sampled at uniformly spaced time intervals, T_s, the output samples, $x[n]$, can be expressed as $x[n]{=}x(t)|_{t=nT_s}$, and are shown in Figure 46 that illustrates a block diagram of ADC,

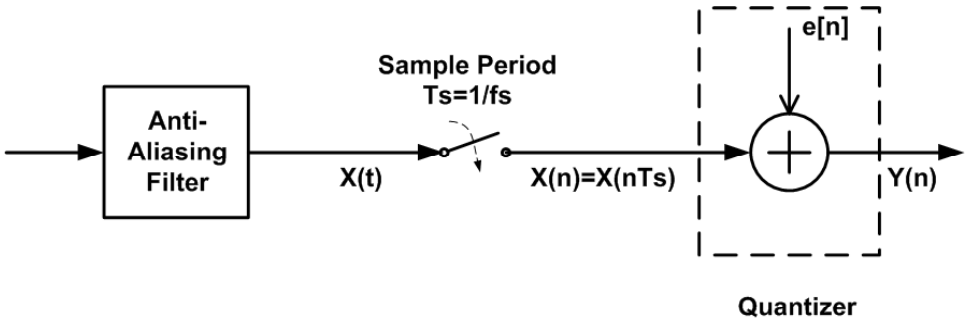

Figure 46: A block diagram of ADC

which consists of an anti-aliasing filter, a sampler, and a quantizer. The quantizer is a nonlinear component that approximates the analog input value with a discrete value of limited precision. The relationship between input and output of quantizer is:

$$y[n] = x[n] + e[n], \tag{14}$$

where e[n] is the quantization error sequence. To simplify the analysis, the following assumptions about the quantization error sequence are made: 1) it is a stationary random process; 2) it is uncorrelated with $x[n]$; and 3) the quantization error is a white noise.

In signal processing, there is a well-known theorem for sampling a bandlimited analog signal, which can be stated as: in order to exactly reconstruct the the original analog signal, which has all frequency components under a frequency f_{max}, from the samples, it is required that the sampling rate f_s is at least two times the frequency f_{max}, that is, $f_s \geq 2f_{max}$. Otherwise, there will be frequency overlaps in the frequency spectrum of the sampled signal, thus it is impossible to reconstruct the original signal through filtering. The sampling rate f_s $(= 2f_{max})$ is called the Nyquist Rate. Figure 47 shows the process.

After the original signal is sampled, the output is mapped from the analog domain to the digital domain through the quantization process shown in Figure 48. The quantized output is represented by a digital code word with N-bit resolution, referring to 2^N reference levels. In the process of quantization, the analog input is approximated by the closest reference level in the output, and the approximation or "rounding" effect will create the quantization error illustrated in Figure 49.

If V_{ref} denotes the full scale analog input voltage, then the minimum resolvable analog input change, denoted as $\triangle$, that can generate a change in the output digital code word, is $\triangle = V_{ref}/2^N$ and corresponds to the least significant bit (LSB) of the output digital code. The quantization error, denoted as σ_e, can be treated as a white noise called quantization noise, if the following assumptions hold: 1) it is an

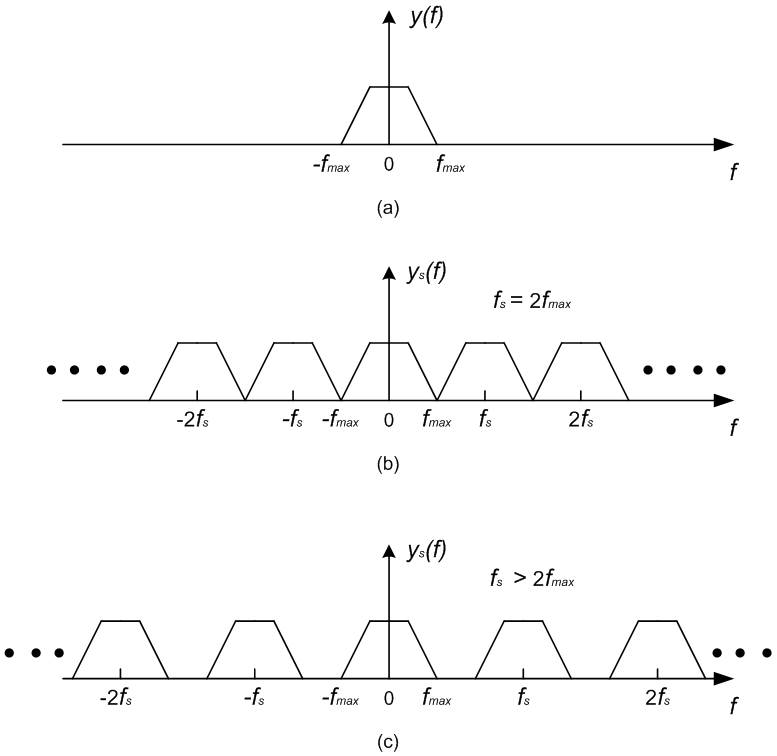

Figure 47: a)spectrum of a bandlimited analog signal to be sampled; b)spectrum of the sampled signal with $f_s = 2f_{max}$; c) spectrum of the sampled signal with $f_s > 2f_{max}$

independent random variable uncorrelated with the analog input; 2) it is uniformly distributed over the range [-$\triangle$/2, +$\triangle$/2]. Under those assumptions, the quantization noise power may be expressed as:

$$\overline{\sigma_e^2} = \int_{-\triangle/2}^{+\triangle/2} \sigma_e^2 \, d\sigma_e = \frac{\triangle^2}{12}, \tag{15}$$

The power of the input signal is $\sigma^2 = V_{ref}^2/8$ assuming that the input signal is a sinusoid with the peak-to-peak value of V_{ref}. Thus the signal to quantization noise ratio can be expressed as:

$$SNR(dB) = 10 * \log_{10}(\frac{\sigma^2}{\sigma_e^2}) = 6.02 * N + 4.77(dB). \tag{16}$$

Equation (16) shows that for every 1 bit resolution improvement, an increase of 6.02 dB in SNR is required. This equation is generally used to translate the SNR

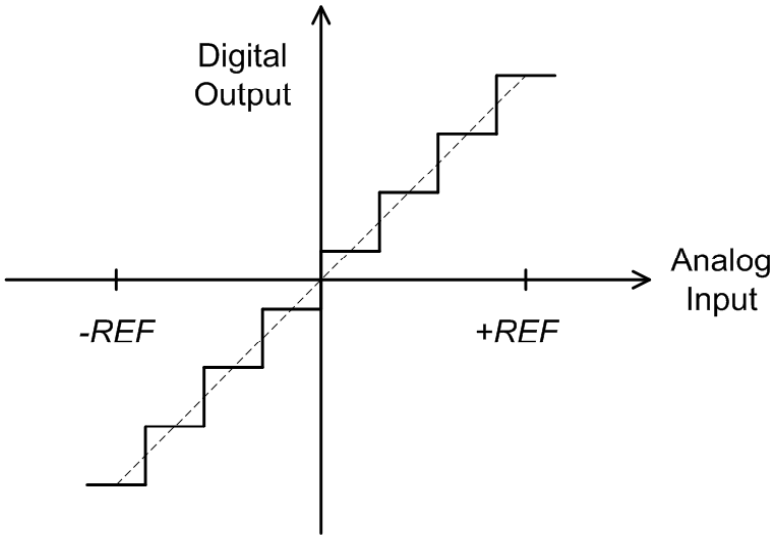

Figure 48: Transfer of the sampled signal to the limited output levels.

into N-bit accuracy, called effective number of bits (ENOB), in both Nyquist and oversampling ADCs.

The Nyquist ADC has the advantage on the applications where ultra-wide input signal bandwidth is an essential requirement, and the restrictions on power consumption and AD conversion resolution (usually lower than 8-bit) can be relaxed. For the high-resolution AD conversion, the number of some building components is exponentially increased, and makes the realization difficult due to the restriction of VLSI technology. Moreover, to achieve high-resolution AD conversion, some extra techniques or components, such as laser trimming technique and anti-aliasing filter with sharp cut-off, are needed. All these requirements make the realization of high-speed, high resolution Nyquist ADC very expensive and almost impossible when power consumption is also a factor to be considered. A relatively less demanding alternative method to achieve high-resolution AD conversion is to oversample the bandlimited signal with a sampling rate much higher than the Nyquist rate, and is discussed in more details in the following sections.

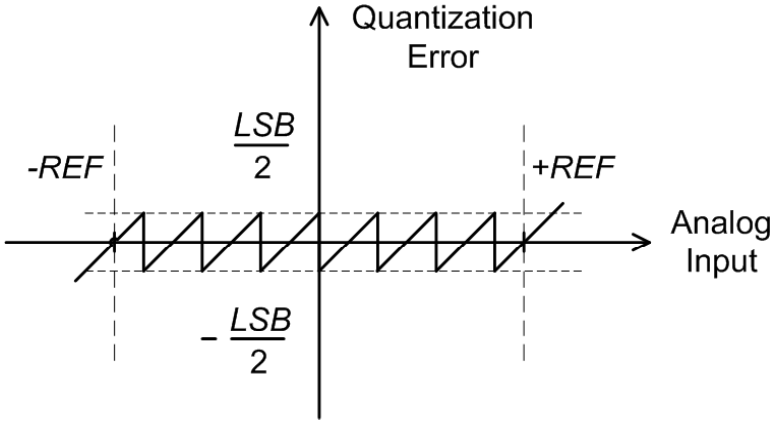

Figure 49: Quantization errors in the AD conversion

4.1.2 Oversampling ADC and Its Operation

In oversampling AD conversion, the sampling rate is much higher than the Nyquist. As a result of increased sampling rate, total quantization noise power is distributed over the spectral range [-f_{s2}/2, +f_{s2}/2], compared to the spectral range [-f_{s1}/2, +f_{s1}/2] in the case of Nyquist sampling, where f_{s1} is the Nyquist sampling rate, f_{s2} is the oversampling rate, and note that $f_{s2} >> f_{s1}$. With the same amount of quantization noise power for both Nyquist ADC and oversampling ADC, The quantization noise power that falls inside the signal band and corrupts the desired signal is reduced in the oversampling case due to the spread noise spectrum, as shown in Figure 50.

In the case of oversampling conversion, the quantization noise power in the signal band, denoted as σ_{e2}^2, is expressed as follows:

$$\begin{aligned} \sigma_{e2}^2 &= \int_{-\frac{f_{s1}}{2}}^{\frac{f_{s1}}{2}} P_{e2}(f)df = \int_{0}^{\frac{f_{s1}}{2}} 2 * P_{e2}(f)df \\ &= \int_{0}^{\frac{f_{s1}}{2}} 2 * \frac{\sigma_e^2}{f_{s2}}df = \sigma_e^2 / \left(\frac{f_{s2}}{f_{s1}}\right) = \sigma_e^2/OSR, \end{aligned} \tag{17}$$

where $P_{e2}(f)$ is the power spectral density for the quantization noise in the output of

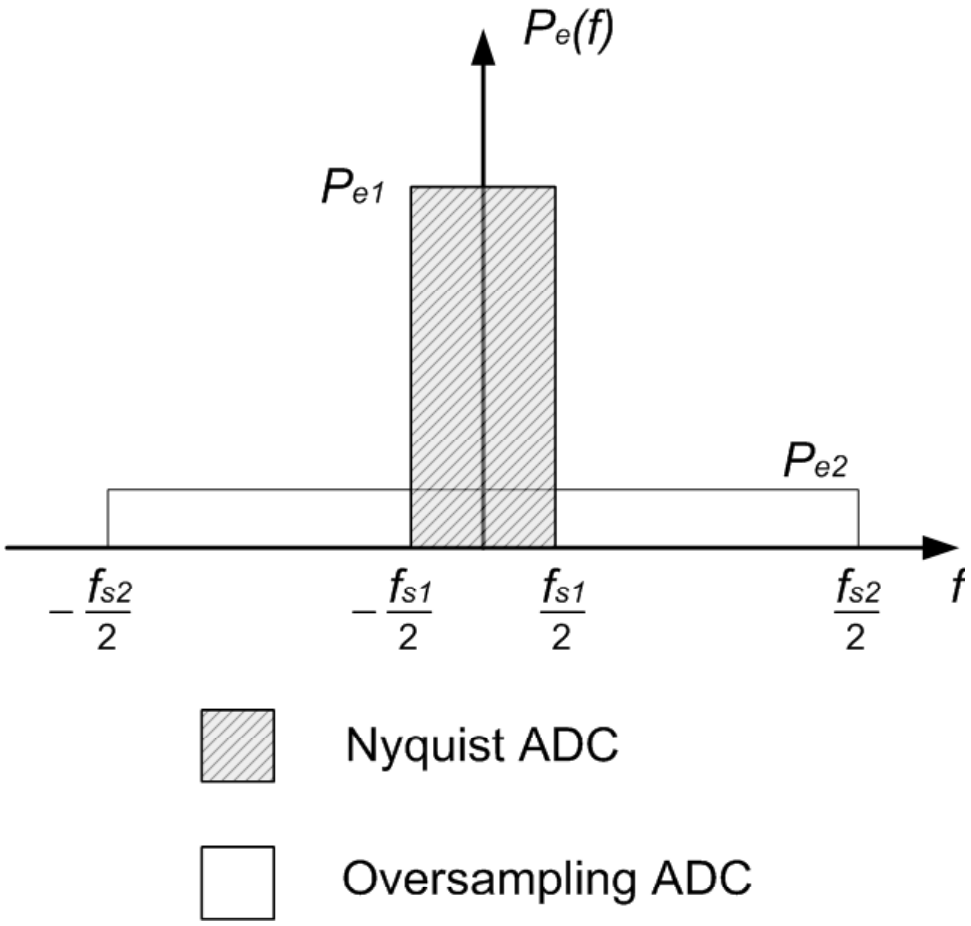

Figure 50: Quantization noise spectrum: Nyquist sampling ADC and oversampling ADC

oversampling AD modulator, and OSR, short for the oversampling ratio, is defined as the ratio between the sampling rate (f_{s2}) and Nyquist rate (f_{s1}), and is written as follows:

$$OSR = \frac{f_{s2}}{f_{s1}} = \frac{f_{s2}}{2f_B}, \tag{18}$$

where f_B is the upper frequency limit for the signal band. If we assume that the desired signal power in the output remains unchanged, then the SNR (dB) is:

$$\begin{aligned} SNR &= 10\log\left(\frac{\sigma^2}{\sigma_{e2}^2}\right) = 10\log\left(\frac{\sigma^2}{\sigma_e^2/OSR}\right) \\ &= 10\log\left(\frac{\sigma^2}{\sigma_e^2}\right) + 10\log\left(OSR\right). \end{aligned} \tag{19}$$

If $OSR = \frac{f_{s2}}{2f_B} = 2^r$, one can derive the following formula from equation (19):

$$SNR = 10\log\left(\frac{\sigma^2}{\sigma_e^2}\right) + 3.01r \quad (dB). \tag{20}$$

It is clear that for every doubling on the OSR, the SNR will improve by around 3 dB, or 0.5 bit translated by equation (16). Note that this derivation is effective in the oversampling ADC system with pulse code modulation (PCM) quantizer.

A block diagram of a first-order $\Sigma\Delta$ AD modulator is illustrated in Figure 51. The modulator is a feedback system that consists of a discrete-time integrator, a quantizer, and a DAC in the feedback loop. This modulator and the digital decimator in the following stage form a complete $\Sigma\Delta$ ADC.

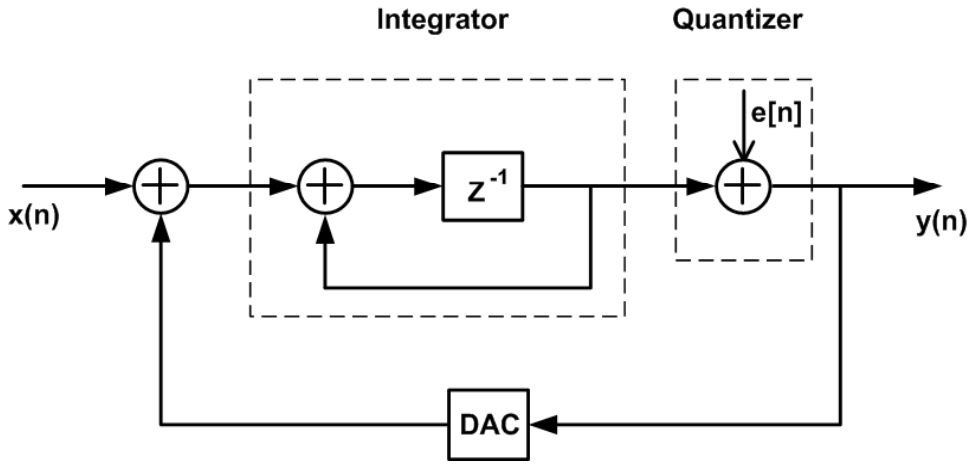

Figure 51: Block diagram of a first-order $\Sigma\Delta$ AD modulator

The equation that describes the operation of the first-order system is written as:

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z) \tag{21}$$

$$= STF(z) * X(z) + NTF(z) * E(z), \tag{22}$$

where STF(z) and NTF(z) are the signal transfer function and the noise transfer

funtion, respectively, and are written as:

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{23}$$

$$NTF(z) = \frac{1}{1+H(z)}, \tag{24}$$

4.2 ΣΔ Modulator Design

In this chapter, a new high-speed second-order, low-pass AD ΣΔ modulator using SiGe HBT technology is presented. Measurements show that the modulator can operate at the 20 GS/sec sampling rate with a good SNR and much lower power consumption compared to III-V implementations [38][46], and with much wider input bandwidth and higher sampling rate compared to CMOS implementations [32]. This work shows that SiGe HBT technology can provide a viable path to low-cost, high-integration, ΣΔ ADCs for use in emerging RF receiver applications.

4.2.1 System Design for the ΣΔ Modulator

A second-order loop filter was chosen for this modulator. For a non-return-to-zero (NRZ) DAC, the noise transfer function can be expressed as:

$$NTF(z) = (1-z^{-1})^2, \tag{25}$$

Based on equation (24), the loop filter $H(z)$ can be derived as:

$$\begin{aligned} H(z) &= \frac{-2z+1}{(z-1)^2} \\ &= \frac{-2}{z-1} + \frac{-1}{(z-1)^2}, \end{aligned} \tag{26}$$

The loop filter H(z) expressed in z domain in equation (26) can be transformed into s domain with a continuous-time expression through the transformation table in [44]:

$$H(s) = -\frac{1+1.5s}{s^2}. \tag{27}$$

Shown in Figure 52 is the the equivalent system level block diagram of the second-order ΣΔ modulator with a loop filter H(s) expressed in equation (27).

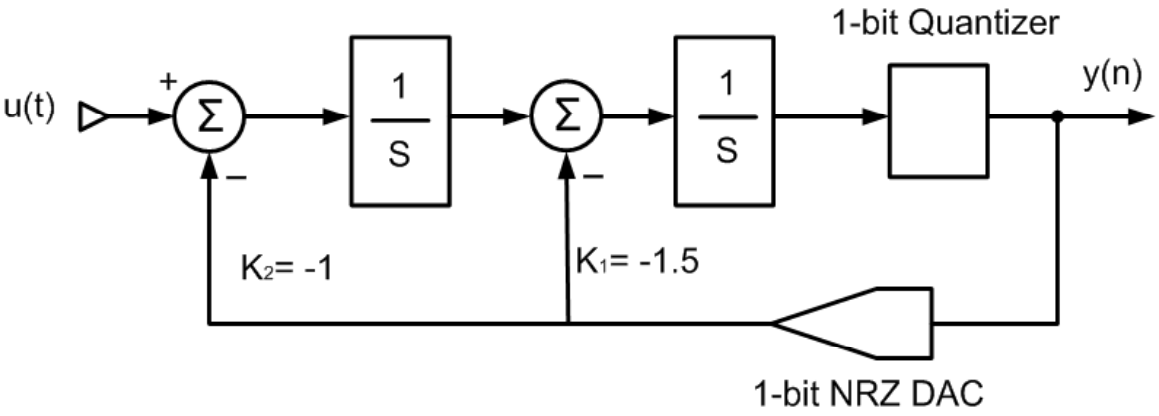

Figure 52: System level block diagram of a second-order ΣΔ AD modulator.

4.2.2 Circuit Design for the ΣΔ Modulator

The block diagram of this SiGe modulator is shown in Figure 53. It is a second-order ΣΔ AD modulator composed of a second-order low-pass loop filter, a master-slave (M/S) comparator, a D-type flip-flop, and two 1-bit digital-to-analog converters (DAC). The second-order low-pass filter consists of two cascaded first-order filters, each of which has a transconductance amplifier followed by an integrator. In the design of the modulator, a highly linear transconductance amplifier (g_{m1}) is desired since the modulator's overall linearity is largely determined by its input stage. A $multi-tanh$ transconductance circuit, designed to achieve high linearity and wide input dynamic range, is shown in Figure 54. The $multi-tanh$ transconductance amplifier achieves a constant G_m over a much wider input dynamic range when compared to a differential pair with emitter degeneration, and is relatively insensitive to the device mismatch in the transistor pairs. In addition, the G_m is linearly proportional to the tail current I_{E2}, which makes it easier to tune the G_m at different stages of the

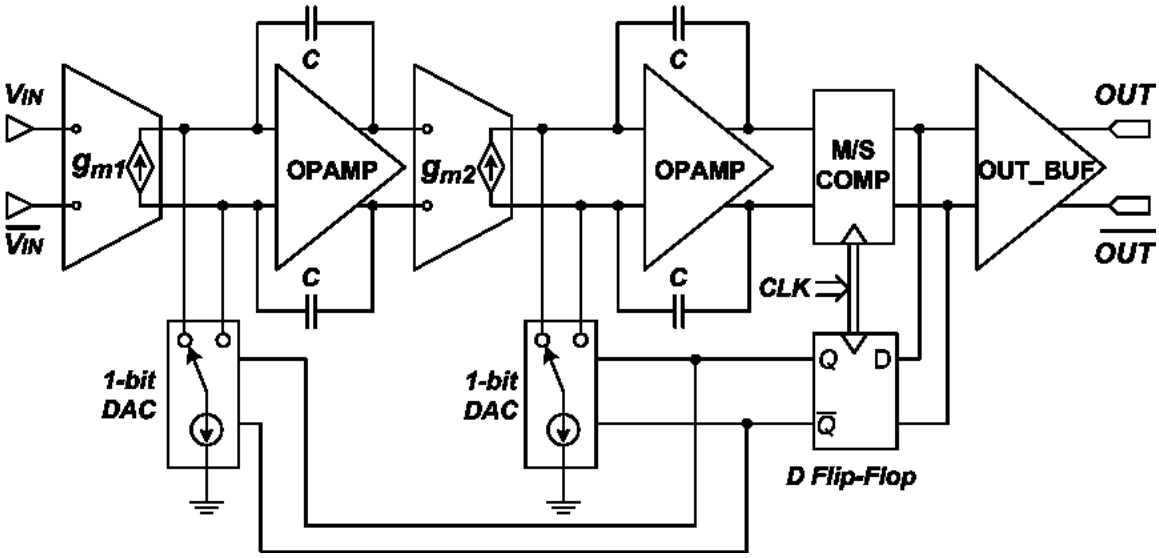

Figure 53: Block diagram of a second-order 20 GS/sec ΣΔ AD modulator.

loop filter. In Figure 54, the transconductance amplifier drives differential current loads that have high differential-mode impedance (for differential signals) and low common-mode impedance (for bias current). The resistors R_{E1} are used to improve the differential-mode impedance: when the voltage in the lower terminal of R_{E1} turns higher, through the loop consisting of transistors Q6, Q8, Q7, and Q5, the voltage in the upper terminal of R_{E1} also turns higher, and vice versa. Therefore, the current flowing through R_{E1} will remain relatively constant with the voltage variations at the output terminals.

In the modulator, the comparator is a critical component that determines modulator's in-band noise, its final resolution, and sampling rate. The master-slave comparator used in the modulator consists of a preamplifier and two cascaded ECL latches implemented by regenerative circuits. Shown in Figure 55 is its schematic.

A differential sine wave signal is fed into the chip and transferred into a square wave clock signal on chip through a clock buffer to drive the comparator. A D flip-flop is used in the feedback loop to reduce the comparator's metastability and adds a

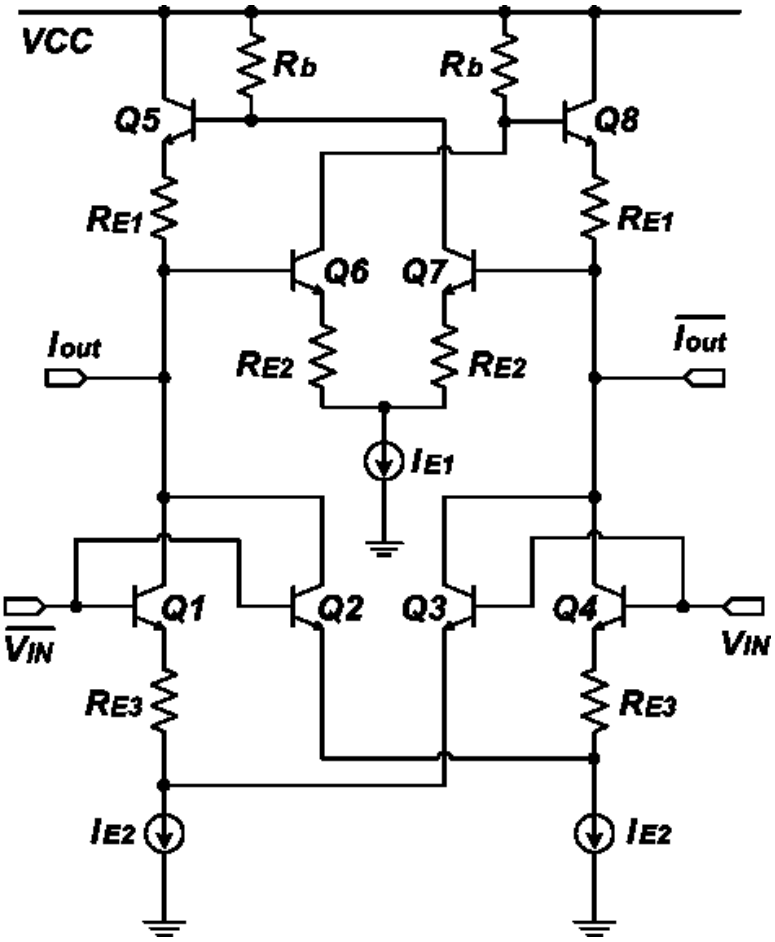

Figure 54: Simplified schematic of transconductance amplifier.

half clock period delay to the feedback signal, followed by two 1-bit current-steering return-to-zero (RZ) DACs. Figure 56 shows the simplified schematic of low-pass filter used in the feed-ward loop of the modulator.

4.3 Measurement Results

The chip micrograph of the modulator is shown in Figure 57. The overall die size, including bondpads, is 1.58 x 1.7 mm^2. On-wafer measurements of the THA were performed using 40 GHz probes and cables. Hybrids were used to split the single-ended input signals into differential signals. Phase tuners were used to adjust the

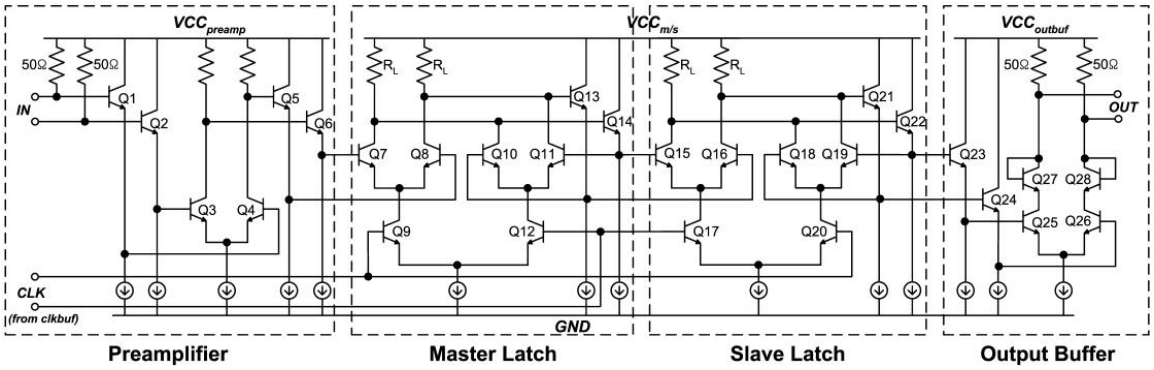

Figure 55: The simplified schematic of the comparator integrated in the modulator.

phase of the cables to exactly 180° phase difference after passing through the hybrid.

In the on-wafer measurements, a 20 GS/sec clock signal was used to drive the modulator. The input was a 312.5 MHz differential signal. The oversampling ratio (OSR) is 32. The frequency spectrum, from 10 MHz to 1.6 GHz, of the modulator's digitized output was measured with a spectrum analyzer, and is shown in Figure 58. The output bit stream eye diagram can also be seen with a wideband oscilloscope, and is shown in Figure 60. The output spectrum from DC to 2 GHz is shown in Figure 59 with the input power increased from -23 dBm to -14 dBm while other test conditions kept unchanged.

Figure 61 shows the measured SNR versus input power over the frequency spectra of 1 MHz and signal band from DC to 312.5 MHz. The input power in the plot is normalized to the maximum stable output of the first DAC in the feedback. The test results for the maximum SNRs for those two spectra are 51 dB (8 bits) and 30.5 dB, respectively.

The modulator operates off a single 3.5 V power supply and dissipates a total power of 490 mW. Table 11 shows a performance comparison of $\Sigma\Delta$ modulators operating in the GS/sec range. The present modulator demonstrates a good SNR and much lower power consumption compared to other III-V AD modulators, and

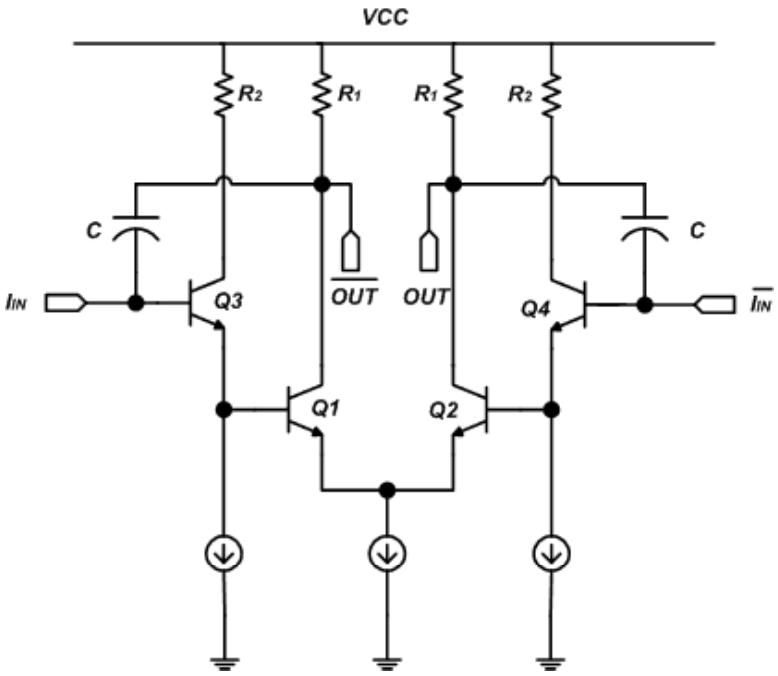

Figure 56: The simplified schematic of the low-pass filter.

has much wider input signal bandwidth than that achieved by CMOS AD modulators. This work was presented at IEEE Custom Integrated Circuits Conference 2006 [88].

Table 11: Performance Comparison of Low-Pass ΣΔ Modulators Operating in GS/sec.

Reference	clock/f_{in} [GS/sec/MHz]	SNR/BW [dB/MHz]	Power Supply [V]	Power [mW]	Technology [-/f_T in GHz]
This work	20 / 312.5	51 / 1.0	+3.5	490	SiGe / 200
[38]	3.2 / 50	71 / -	+/- 5	1000	InP / 70
[46]	18 / 150	48 / 0.01	-	1500	InP / 200
[32]	2 / 2.5	79 / 1.23	-	18	0.18 μm CMOS

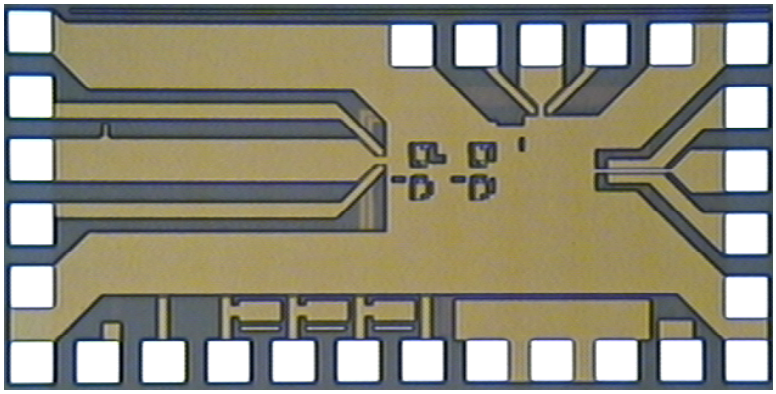

Figure 57: Die photo of the second-order ΣΔ AD modulator.

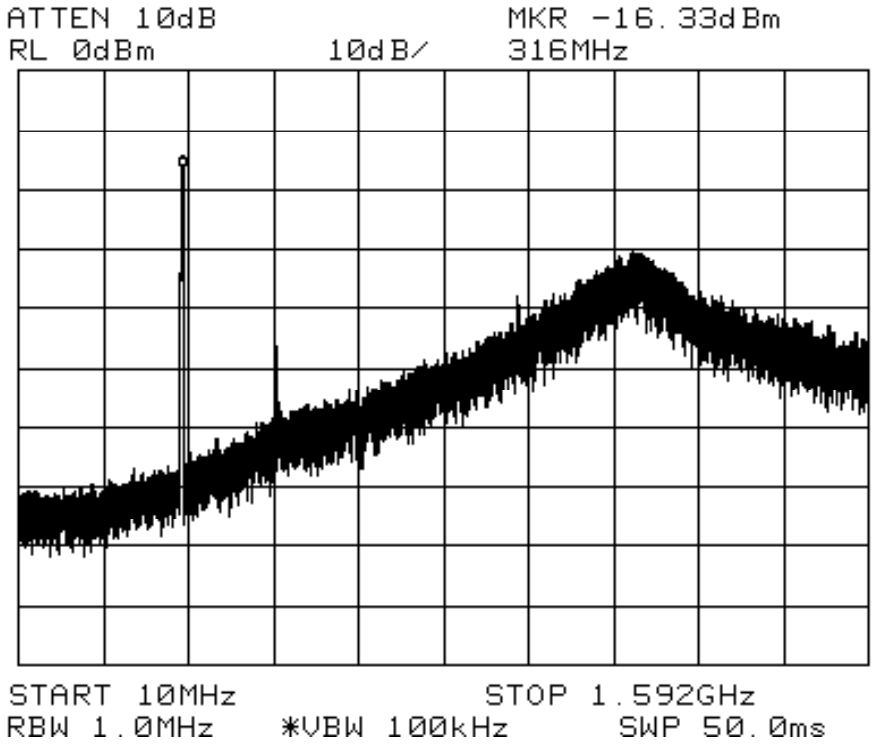

Figure 58: The measured output spectrum from 10 MHz to 1.6 GHz with a sampling rate of 20 GS/sec, and an input signal of 312.5 MHz frequency and -23 dBm input power.

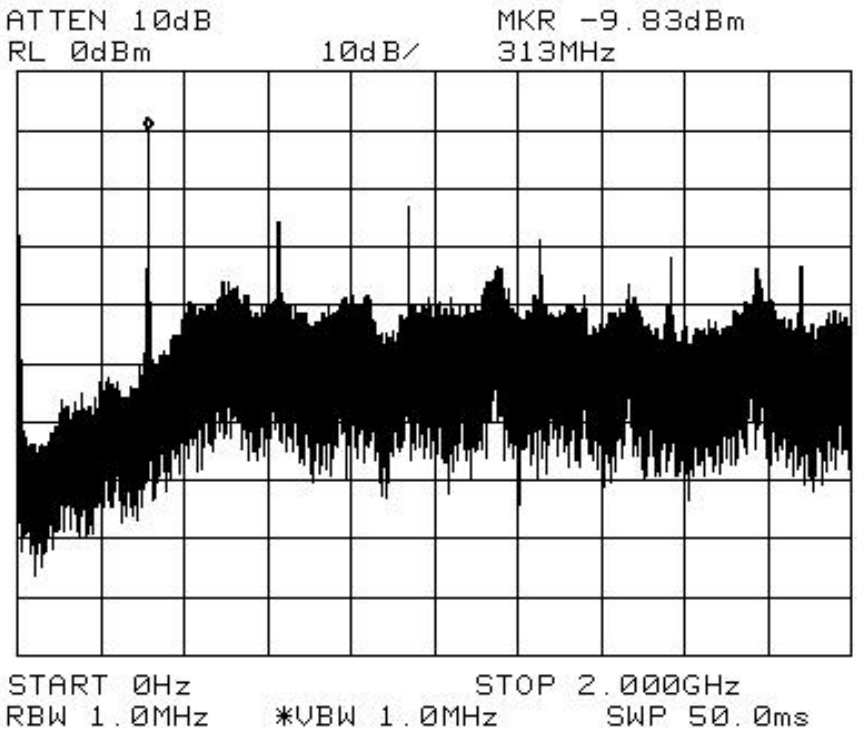

Figure 59: The measured output spectrum from DC to 2.0 GHz with a sampling rate of 20 GS/sec, and an input signal of 312.5 MHz frequency and -14 dBm input power.

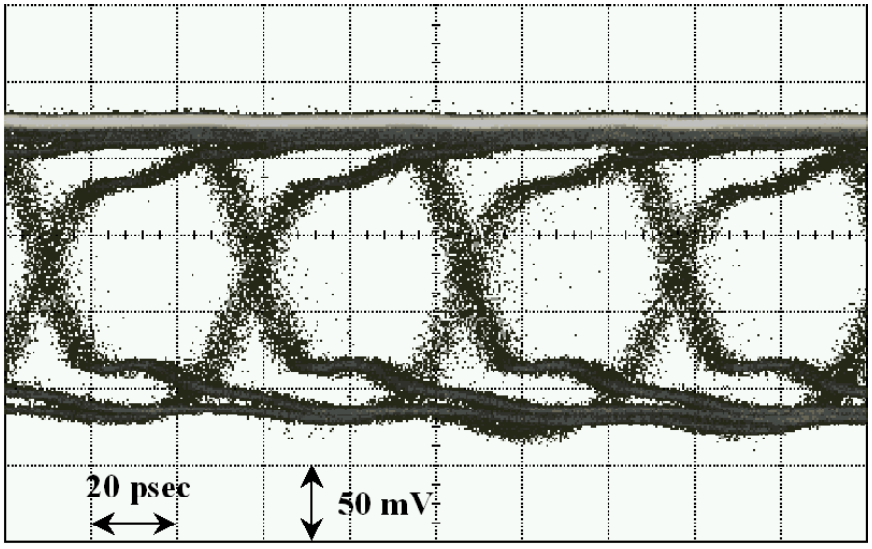

Figure 60: The modulator's output eye diagram with 20 GS/sec sampling rate and 312.5 MHz input signal.

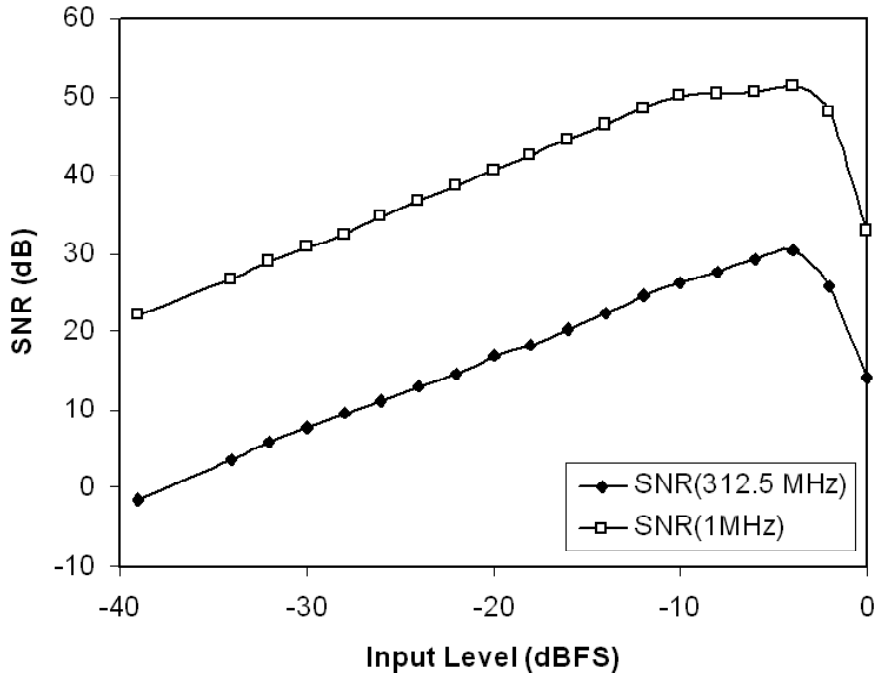

Figure 61: Measured output SNR over the bandwidths of 1 MHz and 312.5 MHz, with 20 GS/sec rate and 312.5 MHz input signal.

CHAPTER V

CONCLUSIONS AND FUTURE WORK

The contributions in this research are summarized as follows:

1. Two ultra-high-speed monolithic comparator were proposed and implemented with SiGe HBT technology. Using master-slave structure and ECL configuration, the comparators demonstrate the fastest sampling rate up to 32 GSamples/sec, and up to 30 GSamples/sec when operating at Nyquist. On-wafer measurements show that the comparators achieve the best input sensitivity-sampling rate combination when compared with other stand-alone comparators in literature.

2. Two ultra-high-speed track-and-hold amplifiers (THAs) were proposed and realized with SiGe HBT technology. The first SiGe THA demonstrates a medium accuracy at the sampling rate of 18 GSamples/sec, and a very low-power characteristic that makes it well-suited for the ADCs in radio mobile communications. The second SiGe THA employs the feedthrough attenuation network originally proposed to suppress the signal-dependent non-linear feedthrough interference suffered by the conventional THAs. Compared with the THAs published in literature with the operational range from 10 GS/s to 20 GS/s, the present THA demonstrates a THD comparable to the best achieved to date in Si technology, with much improved high-frequency characteristics. On the other hand, in the operational range of 30 GS/s and above, the present SiGe THA still exhibits robust characteristics compared with the fastest THAs in terms of linearity, power consumption, and sampling rate.

3. A monolithic continuous-time second-order AD $\Sigma\Delta$ modulator implemented with a 200 GHz SiGe HBT technology was designed and measured. The modulator can operate at a sampling rate of 20 GS/sec with SNRs of 30.5 dB over a signal band from DC to 312.5 MHz, and 51 dB over 1 MHz bandwidth. The present modulator demonstrates a good SNR and much lower power consumption compared to other III-V AD modulators, and has much wider input signal bandwidth than that achieved by CMOS AD modulators.

In the future, this work could be extended in the following directions:

1. Design a bandpass AD $\Sigma\Delta$ modulator to directly sample the high-frequency signal in the range of GHz.

2. Utilizing the THA and comparator implemented in this work, build a high-speed folding/interpolating ADC operating at the rate above 20 GSamples/sec, or a flash ADC operating at the rate above 50 GSamples/sec. The emerging SiGe HBT technology with a cutoff frequency f_T above 350 GHz is very critical to the realization of the ADCs. The comparator's metastability probability, a key parameter for ADCs operating at the rate above 10 GSamples/sec [60], can be reduced with an increased f_T [19]. THA's bandwidth and sampling rate will also benefit from the HBTs' high f_T. With high-speed high-performance THA and comparator available, it is possible to realize a time-interleaved flash ADC with a resolution of 5 bits and a sampling rate up to 60 GSamples/sec, as discussed in [89]. In addition to the challenges on the design of individual building blocks, huge challenges are expected on solving the problems such as various mismatches (timing, offset, etc.), power consumption, thermal issues, and measurements.

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